# A THREE-DIMENSIONAL BIDIRECTIONAL INTERFACE FOR NEURAL MAPPING STUDIES

**by**

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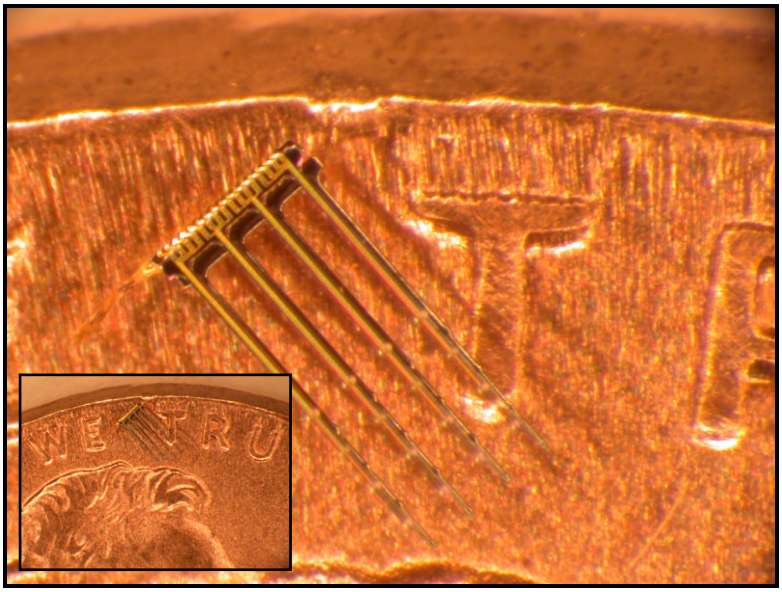


Proverbs 3:5-6

To Jesus, my All in All

To my parents, Dan and Bernice Merriam
To my brothers, Thomas and Aaron

To all of my Sisters of the
Dominican Sisters of Mary, Mother of the Eucharist

## ACKNOWLEDGEMENTS

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The Dominican Sisters of Mary, Mother of the Eucharist, my religious Community, gave me the spiritual support and encouragement to persevere over the past three years; I thank all of them for their witness, sacrifices, and prayers. In particular, I would like to thank the Council, Mother Assumpta, Sister Joseph Andrew, Sister Mary Samuel, and Sister John Dominic, for the opportunity to complete my degree within the context of our religious life. My gratitude also goes to the Prioress, Sister Maria Faustina, for her support as well as to the Sisters who directly assisted in the research, especially Sister Annunciata and Sister Maria Rosario.

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Above all, I thank God for His abundant gifts.

## PREFACE

## A SISTER IN SCIENCE

Upon returning to the University of Michigan to complete my degree, I was not infrequently asked why I was on campus and what I was studying. The answer was at times received with surprise, a smile, a questioning look, a wish for success, and often with a wonder of the unexpected. The question was left lingering – why would a religious Sister be in a field related to science and technology? How grateful I am to have had this opportunity to study electrical engineering at the University of Michigan and how thankful for the warm welcome I received from faculty, staff, and students alike. Out of this gratitude and the positive experience of my studies, I would like to take this opportunity to reply to those who wonder and want to know more about my presence in this field.

The material world, created by God and declared by Him as good[1], is one of the first ways He reveals to humankind something of himself. [2] As Pope Benedict stated:

> A man of faith and prayer…can cultivate serenely the study of the natural sciences and progress in the knowledge of the micro and macro cosmos, discovering the laws proper of matter, because all this concurs to feed the thirst for and love of God.[2]

This thought was also manifested by Pope John Paul II, who said "this witness [of creation] is given as a gift and at the same time is left as an object for study on the part of

human reason.[3]" By "using the steps of creation, man rises toward God by reading the witness of the being, the truth, the goodness and the beauty that creatures have in themselves.[3]" Endowed with intellect and will, mankind's application of his reason to creation deepens his understanding of himself, enables him to better humanity, and allows him to grow closer to his Creator.

Not only can creation lift one's mind to the Creator, but humankind was also commissioned by God, as stewards of the natural creation, to cultivate the world and develop its inherent potential in order to serve the good of humanity and glorify God. One means for this is through the use of technology which "in this sense, is a response to God's command to till and keep the land (cf. Gen 2:15) that he has entrusted to humanity…[4]" Through the complementary nature of science, technology, and faith, the "scientific study is transformed then into a hymn of praise.[2]"

Through the use of the gifts and talents God has given me, I aspire to seek truth, serve others, and glorify God. It is encouraging to me to realize that the Church promotes engagement in the secular sciences and the development of our intellects. It is sometimes presumed that there is a dichotomy between reason and religion. However, truth can not be opposed to itself; "between science and faith there is friendship.[1]" As Pope Benedict commented, "the men of science can undertake, through their vocation to the study of nature, a genuine and fascinating journey of sanctity." It is in part through these means that I endeavor to grow in the both the human and spiritual virtues.

[1]Genesis 1

[2]Pope Benedict XVI, "On St. Albert the Great," address given March 24, 2010, translated and published online by Zenit, http://www.zenit.org/article-28741?l=english

[3]Pope John Paul II, "God, Father and Creator: A Catechesis on the Creed," Pauline Press.

[4]Pope Benedict XVI, "Caritas in Veritate" Encyclical Letter

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## ABSTRACT

**A THREE-DIMENSIONAL BIDIRECTIONAL INTERFACE FOR NEURAL MAPPING STUDIES**

**by**

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**Chair: Kensall D. Wise**

Advances in neuro-medicine depend critically on supporting technologies, including those associated with penetrating microelectrodes. While these have developed from single-site microwires to three-dimensional micromachined electrode systems, several important issues remain. This research focused on the array-tissue interface, on application-specific electrode design, and on neural amplifiers for use in bidirectional microelectrode system front-ends.

Three new three-dimensional array structures were developed. A novel architecture, which enables two perpendicular probe sets, was coupled with open-scaffold shanks to create 3-D lattice arrays for bio-response investigations. These arrays have 15% of the shank area of constant-footprint solid counterparts. Chronic (8-week) *in vivo* studies have shown similar 2-D lattice probes significantly mitigated the tissue reaction and dramatically increased the number of adjacent (within 50μm) surviving neurons from 36% to 87%.

An innovative design for rapidly-assembled folded 3-D arrays was created, requiring only one mask beyond the standard boron-doped process. This realizes the smallest platform structure ever reported for such a device, with zero-rise above the platform top and virtually no lateral extent past the probes. Electrode and shank pitch are both 200μm on the 64-site prototype. The implanted device stands less than 350μm above the cortex and displaces only 1.7% of the instrumented area. Recordings in guinea pig cortex verified functionality.

A 160-site array for neuroscience mapping of the ventral and dorsal cochlear nucleus consisting of five-probes (3-VCN, 2-DCN) permitted high-density 3-D CN mapping and somatosensory integration studies for the first time. Multi-region stimulation (1000μm2 sites) and recording (177μm2 sites) demonstrated the efficacy of bimodal silicon arrays for investigating the biological circuits of the central nervous system and as prosthetic devices.

For electrode-electrolyte interface enhancement, iridium sites were modified with carbon nanotubes (CNTs). On non-released probes, in situ growth of vertically-aligned forests was achieved, and dip-coated sites exhibited an order-of-magnitude impedance reduction. Neural signals in guinea pig cortex were recorded with released dip-coated CNT-probes.

A new integrated neural recording amplifier, consuming only 46.5μW of power, was designed and fabricated in a 0.5μm CMOS process. The 0.026mm2 circuit has an in-band gain of 58.9dB with a tunable lower cutoff frequency and an upper cutoff frequency of 21.3kHz.

# CHAPTER I

# INTRODUCTION

Advances in medical science have not only expanded our knowledge of neural anatomy and physiology, but have also enabled breakthroughs in the care of patients with debilitating conditions such as deafness and Parkinson's disease [1]. Developments already achieved are an indicator of the potential for future progress. However, the fields of biomedical research and health care travel in parallel with engineering innovations. Microelectrodes are one of the supporting technologies that have facilitated study of the central nervous system and the treatment of its disorders. Since their inception, engineering enhancements in the design and fabrication of microelectrode devices have continued and have broadened to include entire microelectrode systems. These devices and systems, utilized as research tools, enable the neuroscience community to ask and answer questions beyond the scope of previous methodologies. They also offer novel approaches to restoring lost function in the form of prospective medical prostheses.

## 1.1 Initial Approaches to Interfacing with Neurons

Electrodes form the interface between signals carried by electrons in a conductive solid and those carried by ions in extracellular fluid. Neural signals, single and multi unit activity as well as local field potentials, can be recorded from the voltage waveform at the electrode surface and neurons can be stimulated through the electrode using either a voltage or current protocol [2]. The first types of electrodes used *in vivo*, glass micropipettes and metal microwires, are still in use today. The simplest of these have one electrode site at the tip of the device. A small device diameter is desired to minimize insertion trauma. While these types of electrodes are commercially available, many laboratories also make them by hand, and the actual production has become an art. Various means are used to ensure small electrode site size. Lack of reproducibility is one drawback. Another shortcoming is the inherent limitation of only one site and one

interconnect lead per device. This has been confronted by several approaches in order to form two- or three-dimensional arrays. However, reproducibility remains an issue. Another difficulty is that once the number of sites becomes large, the volume of tissue displaced becomes significant. Other challenges also exist such as a lack of clear knowledge of relative site positions, the splaying of sites during insertion (for wire bundles), and the lack of accurate control of site size. In spite of these obstacles, many researchers continue to use these devices. This may be due to their ready availability and traditional usage. However, other technologies have been developed which alleviate many of the challenges inherent in these first-generation electrodes.

## 1.2 Micromachined Electrode Arrays and Systems

Over the past several decades, significant work has been undertaken in various institutions to further develop microelectrode arrays and systems for use in neuroscience research and medical applications.

### 1.2.1 History of Micromachined Electrode Arrays

The electrical engineering field made major advances with the development of photolithographic technology, which enables batch fabrication of integrated circuits. In the mid 1960's at Stanford University, Kensall D. Wise and James B. Angell applied this technology to biomedical devices to form an array of electrodes [3]. This innovation opened a door to future electrode array development as well as to the field of micromachining [4]. Fig. 1.1 shows a drawing and photomicrographs of a single electrode microprobe; multielectrode microprobes were also fabricated.

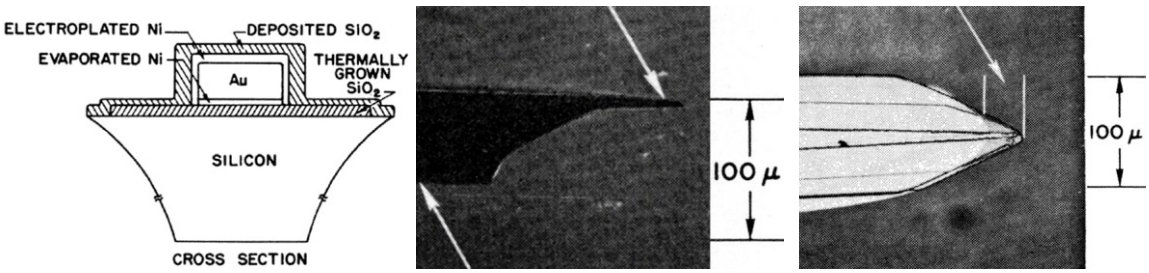



Fig. 1.1: Single electrode microprobe (a) cross sectional drawing and (b) side view and (c) top view photomicrographs, cropped from [3].

The next logical step was to combine micromachined electrode arrays with circuitry. In 1971 and 1975, Wise and Angell reported hybrid devices consisting of multielectrode probe structures and integrated circuit chips for multichannel buffering of the recorded neural signals [5, 6]. These structures maintained the location of the electrode sites at the tips of the protruding shanks, but sites designated for recording and for stimulation were both included. Junction Field Effect Transistors (JFET) were used in a source follower topology to reduce channel crosstalk, noise, and output resistance. The possibility of integrating probes and circuitry in the same device was also acknowledged.

At Tohoku University in Japan, Kouro Takahashi and Tadayuki Matsuo developed a fully monolithic approach and in 1984 reported an active probe with MOSFET amplifiers and switches at the probe back-end and multiple electrode sites along the probe shank [7]. Chemical etching was used to shape the probes, but no etch-stop was included for the back-side thinning. In 1985 at the University of Michigan, Khalil Najafi, Kensall Wise, and Tohru Mochizuki reported a boron etch-stop fabrication process compatible with on-chip circuitry [8]. This new process simplified probe fabrication and significantly increased device yield. Najafi and Wise reported a ten channel active probe using enhancement-depletion (E-D) NMOS technology to amplify, multiplex, and self-test in 1986 [9, 10]. Jin Ji and Kensall Wise followed this with a thirty-two site, eight channel, active probe with CMOS circuitry for site selection, signal amplification, and output multixplexing in 1990 [11]. From there, the technology has continued to develop with both hybrid and integrated approaches being explored.

### 1.2.2 Worldwide 2-D Probe Technology

Since the initial application of micromaching to the formation of electrode arrays for scientific and medical use in the brain, the area has developed into a distinct field of research and has been joined by groups worldwide. Subsequently, reviews have also been published covering aspects of the research from anatomical and physiological compatibility, to material selection, to summaries of the numerous structural methods employed [12-18]. Although it is not feasible to exhaustively review the many works in

this field within the confines of this writing, the major approaches can be grouped by fabrication technology, each with its particular advantages and drawbacks.

The University of Michigan has been a leader in the micromachined electrode field with the development of boron-doped silicon probe technology for *in vivo* use. The design and fabrication process flow for passive two-dimensional structures has been well characterized, enabling a large variety of single and multiple shank implants to be made widely available to the neuroscience community through Michigan's Center for Neural Communication Technology (CNCT). Within ten years of its beginning in 1994, CNCT had distributed over 6200 two-dimensional passive probes in approximately 200 different designs, leading to more than 100 papers in neuroscience literature and over 200 conference presentations [19]. With the boron-doped process, virtually any two-dimensional design can be fabricated, and the selective etch-stop enables uniform and multiple thicknesses. However, the boron sources are expensive and not widely used so supplementary and alternative techniques have been developed both at Michigan and elsewhere. Subsequent sections further detail Michigan probe work.

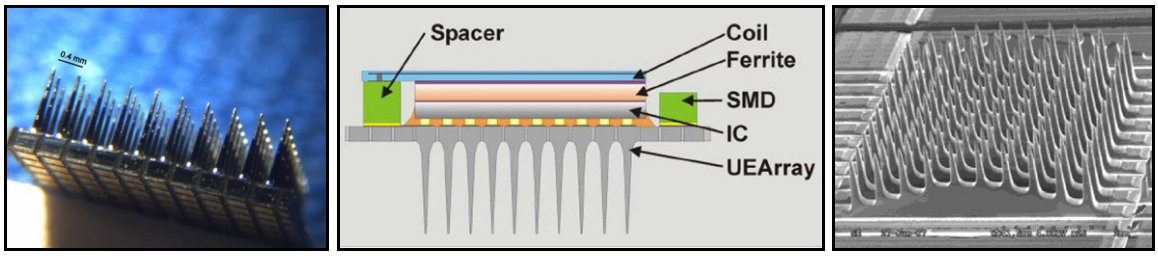
Anisotropic bulk etching of silicon has been employed to shape probes using potassium hydroxide (KOH) with an electrochemical etch-stop [20] or to thin probes with no etch-stop [21]. Another approach combined a front-side plasma etch with timed or visually inspected back-side thinning in KOH [22, 23]. With the development of deep reactive ion etching (DRIE) [24-26], dry etching of silicon became more appealing. This has led to the combination of a DRIE front-side etch and KOH back-side thinning with sidewall protection for increased yield [27]. DRIE has also been used to define the probe shape from both sides [28, 29]. However, challenges are encountered in setting device thickness and obtaining high yield whenever bulk etching is used without a distinct etch-stop. Silicon-on-oxide (SOI) wafers enable the exact device thickness to be set accurately while still using DRIE to remove the bulk silicon [30, 31]. The disadvantages of this technique are the expense of SOI wafers and the chisel tip profile that results.

Several less common substrates have been employed to enable probe fabrication without the facilities required for bulk etching techniques. These have included glass diamond-scribed coverslips [32], laser-cut ceramic substrates [33], and molybdenum supports [34, 35]. However, these lack reproducibility and produce low yield.

A recent research trend has been use of polymers as probe insulators, even replacing the substrate itself. These include polyimide [36-38] and parylene devices [39-41], and the long-term integrity of the insulation properties in a wet environment has been explored [42, 43]. While some authors promote the flexibility of the polymers as a biocompatibility advantage, there has been no conclusive evidence that the difference in flexibility between polymers and other thin substrates is enough to cause a substantial improvement in the immune response. The insertion challenges inherent with a flexible substrate have been addressed by developing insertion tools [36, 44, 45], thicker devices [41], and fluid-filled channels [46], which enable implantation although at the cost of increased initial or sustained tissue displacement.

### 1.2.3 Approaches for 3-D Arrays

Researchers at the University of Utah took an alternative route to array fabrication as shown in Fig. 1.2. They devised a processing method which utilized a dicing saw and chemical etching to form a ten by ten array of silicon needles with shank length dependent upon the starting wafer thickness [47]. Each shank only supports one electrode site at the tip. Therefore, while the array is three-dimensional in shape, the site distribution is on a two-dimensional surface. The initial planar array was followed by a slanted array and by other shapes as well [48]. This work has also achieved flip-chip integration with hybrid circuitry for individual site amplification and spike detection, output channel selection, and wireless transmission of power, clock, and data [49, 50].

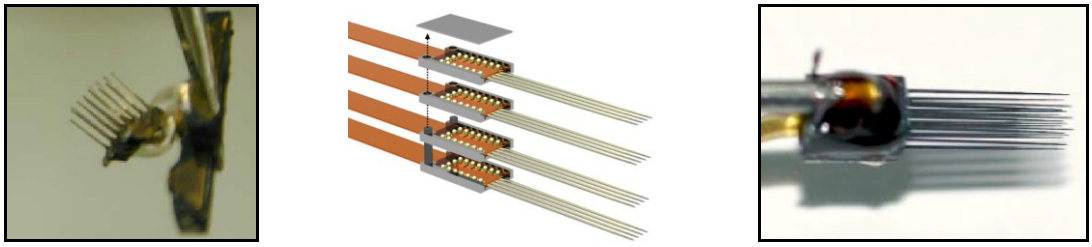



(a) (b) (c)

Fig. 1.2: Arrays developed at the University of Utah (a) optical image of the Utah Electrode Array (UEA), (b) system integration diagram, and (c) cylindrical shaped array [48, 49].

Creating 3-D arrays out of standard 2-D probes is perhaps the first technique that comes to mind for increasing interface dimensionality. Researchers at California Institute

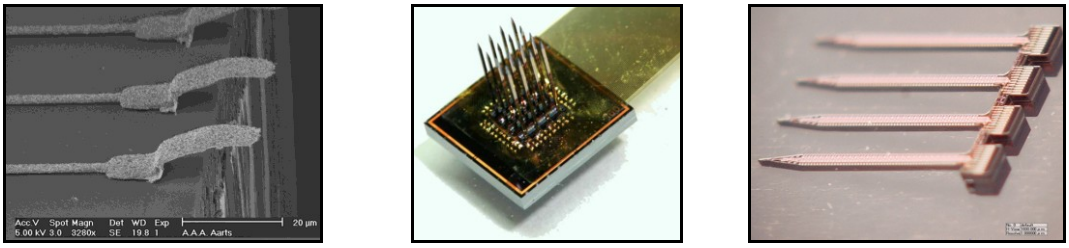
of Technology have formed dry-etched 2-D probes with integrated parylene cables and subsequently formed two-probe and four-probe arrays [28]. A photograph of one device is included in Fig. 1.3. However, the details of their stacking technique were not presented. NeuroNexus Technologies, the Ann Arbor based, University of Michigan spin-off company, has recently expanded to commercially available 3-D arrays. Fig. 1.3 shows the stacking scheme and a photograph of an assembled array. These devices can be customized utilizing a subset of their 2-D chronic probes with up to 128 electrode sites and with probes placed at multiples of 100µm pitch.



(a) (b) (c)

Fig. 1.3: 3-D arrays formed by stacking 2-D probes (a) photograph of a 4-probe stack by researchers at California Institute of Technology [28], (b) conceptual drawing and (c) photograph of a multi-probe stack by NeuroNexus Technologies [51].

In 2006, fourteen groups from across Europe joined together for the NeuroProbes project [52]. This group devised a modular method for incorporating two-dimensional probes into a platform equipped with bays into which the probe back-ends fit; gold beam-lead clips form orthogonal electrical connections between the probes and platform during insertion as shown in Fig. 1.4 [53, 54]. This work also includes site-selection circuitry along the 8mm shanks so that up to eight sites out of 512 on a shank may be chosen [55]. The large back-end thickness constrains the minimum probe pitch to over 300µm.



(a) (b) (c)

Fig. 1.4: Work done under the NeuroProbe project (a) gold beam-lead clips, (b) a 3-D array prototype, and (c) one probe with integrated circuitry [54, 55].

### 1.2.4 Recording and Stimulation Systems at the University of Michigan

As described above, the Michigan technology also combined electrode arrays with circuit functionality. Two approaches have been used, one forming "active" probes with circuitry integrated in the back-end of the probe and a second approach using a hybrid design with ASICs interfacing with passive (or active) probes. Once circuitry was incorporated, the design focus widened to the system level. Two parallel streams of innovation have taken place: recording systems and stimulation systems. These streams reflect the two directions of data transfer, either from the neural cells to the outside world (recording) or from the external setup to the neural tissue (stimulation). Table 1.1 provides information on the most recent recording systems and Table 1.2 on stimulation systems.

**Table 1.1: Selected Michigan Recording System Front-End Circuits**

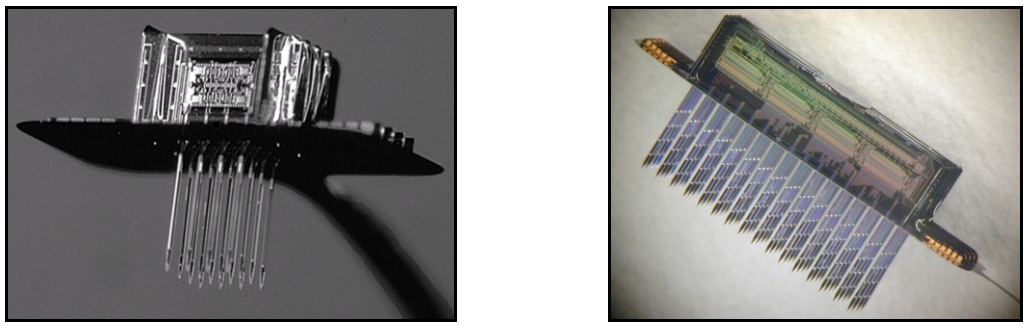
| **Researcher** | **Jamieson [56]** | **Olsson [57, 58]** | **Perlin [59]** |
|---|---|---|---|
| **Date** | 2003 | 2004 | 2008 |
| **Dimensionality** | 2-D | 3-D | 3-D |
| **Site Number** | 64 | 256<br>(4 64-site probes) | 64 |
| **Site Selection** | 64:8 | per probe 64:8<br>24 combinations | Not Included |
| **Amplification** | 0.91 | 1000, in two stages | 100 to 1100,<br>programmable |
| **Bandwidth** | --- | Tunable – 10kHz | Variable – 9.1kHz |
| **Output Multiplexing** | Not Included | 8:1 per probe | Not Included |
| **Input Frame** | 32 bits | 5 bits | 30 bits |
| **External Leads** | 12 (pwr, gnd, data, clk, 8 analog outputs) | 9 (vdd, vss, gnd, clk, rst, mode, adrs, tune, out) | 69 (vdd, vss, data, clk, enable, 64 analog outputs) |
| **Voltage Supply** | 5V | ±1.5V, Gnd | ±1.5V |
| **Circuit** | Integrated | Integrated | Hybrid |
| **CMOS Tech** | 3µm | 2P, 1M, 3µm | 0.5µm AMI |

| Table 1.2: Michigan Stimulation Systems | | | | | |
|---|---|---|---|---|---|
| **Researcher** | | **Tanghe [60]** | **Kim [61]** | **Gingerich [62]** | **Yao [63]** |
| **Date** | | 1992 | 1994 | 2002 | 2005 |
| **System** | | STIM-1 | STIM-2 | STIM-3b | STIM-3 |
| **Dimensionality** | | 2-D | 3-D potential | 3-D | 3-D |
| **Site** | **Area** | Varies | 400/1000μm$^2$ | 1000μm$^2$ | 1000μm$^2$ |
| | **Number** | 16/probe | 64/probe | 64/probe, flexible/array | 64/probe, 1024/array |
| | **Selection** | Not included | 8:1 | 16:1 if 1 probe | 8:1 |
| **Channels** | | 16 | 8 | 4 / system | 8/probe |
| **Current** | **Timing** | External | External | External | External |
| | **Delay/site** | 16 clk cycles | 18 clk cycles | ≥20 clk cycles | 18 clk cycles |
| | **Generation** | On-chip | On-chip | Off-chip | On-chip |
| | **Range** | ±254μA | ±127μA | N/A | ±127μA |
| | **Resolution** | 2μA | 1μA | N/A | 1μA |
| | **Check** | Yes | DAC to pad | N/A | Not included |
| **Recording** | | Not included | One site | Per channel | One site |
| **Electrode** | **Grounding** | Per channel | Per channel | Per channel | Part of bias |
| | **Bias** | 0.65V | Diode drop | External, Per channel | 15 levels, 1 site |
| | **Activation** | Parallel | Yes | Parallel | Parallel, 8/probe |
| | **Impedance** | Pad access | Pad access | Pad access | Pad access |
| **Additional Test & Safety** | | Timeouts, input checks | Trouble flag modes | --- | Site connection test |
| **Input Frame** | | 16 clk cycles | 18 or 36 clks | Varies | 18 or 36 clks |
| **External Leads** | | 5 | 5 | 9 | 7 |
| **Voltage Supply** | | ±5V, ground | ±5V, ground | ±5V, ground | ±5V, ground |
| **Circuit** | | Integrated | Integrated | Integrated | Integrated & hybrid 1.2mm$^2$ |
| **CMOS Tech** | | 1P, 1M, 3μm | 1P, 2M, 3μm | 1P, 1M, 3μm | 2P, 1M, 3μm |
| **Layout Area** | | 11mm$^2$ | 11.2mm$^2$/pr | 7.1mm$^2$/probe | Probe back-end is 22.8mm$^2$ |

Collectively, the Michigan systems have incorporated many features important for chronic wireless bimodality. However, none has been individually capable of fully bidirectional functionality; these systems highlighted one direction and the second was not present or was severely limited. The recording systems do not have stimulation available; the stimulation systems are limited to one or four recording channels.

### 1.2.5 Three-Dimensional Arrays at the University of Michigan

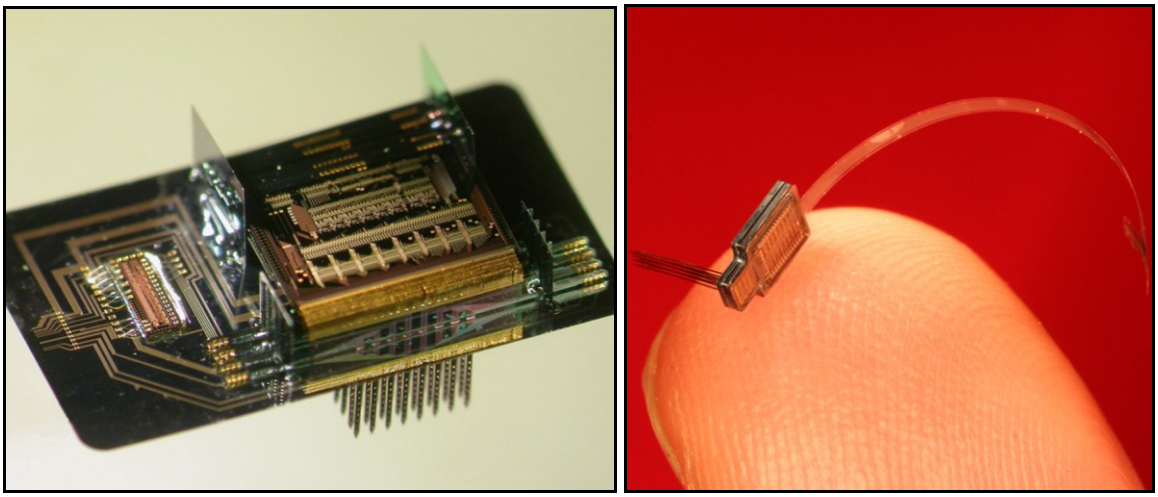
The University of Michigan boron etch-stop probe technology was initially developed for planar two-dimensional implants, but soon expanded to make three-dimensional arrays. The first such structure was developed by Arnold C. Hoogerwerf and was composed of two-dimensional probes inserted orthogonally into a thin platform and held parallel to each other with spacers [64]. The probe back-ends supported flanges with gold contacts; these contacts were electrically connected to corresponding contacts on the platform by electroplating with nickel. The use of a frit glass to seal the platform slots was explored. With Qing Bai's inclusion of circuitry on probe back-ends, the first active three-dimensional recording array was formed, a photograph of which is shown in Fig. 1.5a [65]. She also improved the orthogonal interconnects with the use of ultrasonic gold beam-lead bonding. Marcus D. Gingerich designed an active sixty-four site two-dimensional probe intended for 3-D arrays with a flexible number of probes [62]. A 256-site three-dimensional array was assembled as shown in Fig. 1.5b; a 1024-site array using the same two-dimensional probe design was also assembled. Developments by multiple researchers at Michigan enabled the integration of flexible silicon cables in the device fabrication process [66, 67].



(a) (b)

Fig. 1.5: Photograph of (a) the first active 3-D recording array [65] and (b) an active 256-site 3-D stimulation array [62].

Changhyun Kim and Marcus Gingerich each proposed and prototyped modifying the two-dimensional probes to attain a low-profile design [61, 62]. Work by Ying Yao made this design a reality by modifying the probe back-end so that the circuit portion folded down and latched parallel to the platform; Fig. 1.6a shows an assembled array [63]. As supporting technology for this low profile design, Ying Yao, with the assistance of Ning Gulari, devised a processing method for bendable gold interconnects encased in a parylene encapsulating layer, which led to integrated parylene cables [68]. These devices maintained the use of beam-leads on probe back-end flanges for orthogonal interconnect transfers to the platform. Gayatri E. Perlin simultaneously achieved a low profile structure and simplified the three-dimensional construction [59]. Her structure incorporated probes with beam-leads along the top of the back-end and a full wafer thickness block platform. During assembly, probe back-ends were countersunk in platform slots and the beam-leads were bent flat to the platform and bonded. This strategy removed the need for the horizontal and vertical space-consuming flanges and spacers and left a smooth platform surface for ease in bonding. A three-dimensional array with hybrid circuitry and a parylene overlay cable is shown in Fig. 1.6b. She also worked to decrease the pitch necessary for the beam-lead interconnects.



(a) (b)

Fig. 1.6: Photos of two low profile 3-D electrode arrays in which (a) the integrated circuit portion of the probe back-ends fold down parallel to the platform [63] and (b) the 500µm thick block platform holds probes and a hybrid chip [59].

## 1.3 Research Objectives and Thesis Contributions

The field of implantable micromachined neural electrode array systems has seen remarkable progress since its inception. However, there are still significant obstacles to realizing the full potential of this technology in the neuroscience and medical fields. These include minimizing the reaction of the immune system to the implanted array, enhancing the electrode-electrolyte interface, developing low-power low-area recording amplifiers, and tailoring the specific three-dimensional MEMS construction of the array to selected applications. By focusing on these essential aspects, this work addresses key issues associated with the front-end of a neural recording and stimulation system. Particular goals were:

- To understand the effects of array area on chronic tissue reactions *in vivo*.
- To explore methods for incorporating carbon nanotubes (CNTs) on the electrode sites as a means of decreasing site impedance and potentially improving recording and stimulation capabilities *in vivo*.
- To design an improved neural recording amplifier, the key circuit component in the front-end of a fully-bimodal (record-stimulate) implantable microsystem.
- To develop and test an application-specific electrode array achieving minimal tissue displacement and allowing, for the first time, high-density mapping of the guinea pig anterior ventral cochlear nucleus (AVCN) and dorsal cochlear nucleus (DCN) to enable acute experiments not previously possible and demonstrate the efficacy of mapping using bimodal silicon microelectrode arrays.

Chapter II of this thesis discusses issues related to the chronic neural interface. 2-D and 3-D structures for mitigating the immune response are presented, and results from *in vivo* biocompatibility studies are described. Chapter III focuses on enhancing the electrode-electrolyte interface by incorporating carbon nanotubes on the sites. Process compatible methods for achieving grown or deposited CNTs on the electrodes are discussed with *in vitro* test results of site impedance. Chapter IV discusses the design and test of a neural recording amplifier, highlighting a new low-power and low-area implementation. Chapter V presents a novel 3-D architecture based on a folding scheme which integrates flexible cables with the silicon probes and platform at the layout level. Chapters VI and VII present the design and *in vivo* neuroscience results of an application-specific array for mapping within the guinea pig cochlear nucleus. Chapter VIII summarizes the key contributions of the preceding chapters and makes recommendations for future work.

# CHAPTER II

# STRUCTURAL ENGINEERING OF PROBES TO MINIMIZE TISSUE RESPONSE

Medical investigations, diagnostics, and therapeutic interventions strive to acquire scientific knowledge and/or to restore proper functioning without causing interference with the apparatus employed. However, the presence of foreign objects in the body tends to provoke a response from the immune system. Steps to reduce or eliminate such adverse reactions are essential, particularly for chronic applications. Biocompatibility studies thus possess an important role in the field of implantable medical devices. As a contribution to this field, a series of probes and related structures have been developed for tissue reaction studies. This has been undertaken as part of a collaborative effort with Prof. Patrick A. Tresco (at the Keck Center for Tissue Engineering at the University of Utah) and his laboratory group, in particular Mr. John Skousen, who performed the coatings, *in vivo* implantation, histology, and data analysis. MEMS fabrication was done by Dr. Onnop Srivannavit at the University of Michigan Lurie Nanofabrication Facility (LNF). The probe designs were based in part on previous work done by Dr. Gayatri E. Perlin. This chapter looks at the array-tissue interface and several biocompatibility issues, presents devices developed to further studies in this field, and describes the *in vivo* results obtained with the devices.

## 2.1 Proximate Biocompatibility Investigations

Immune system response is a complex topic with multiple contributing factors. In addition to observing changes in electrode characteristics and array functionality during chronic recording and stimulation, researchers have focused specifically on the brain tissue response to implanted devices through numerous studies [69, 70]. A selection of these bio-response studies are introduced in this section.

The material in contact with the neural tissue is a critical factor in the immune response. Work has been done to compare and classify the reactions due to various materials such as the study by Stensaas, et. al., in which 2-3mm long rods or wedges with diameters of 750μm or less were implanted in the cortex of adult rabbits [71]. Fig. 2.1 presents a drawing of the resulting immune response around the three categories of materials: non-reactive, reactive, and toxic. Gold, platinum, and phosphorus-doped silicon were among the substances classified as non-reactive; silicon dioxide (Pyrex) was placed in the middle category. The severe reaction to some of the implants classified as toxic, such as silver, underlines the importance of biomaterial studies.

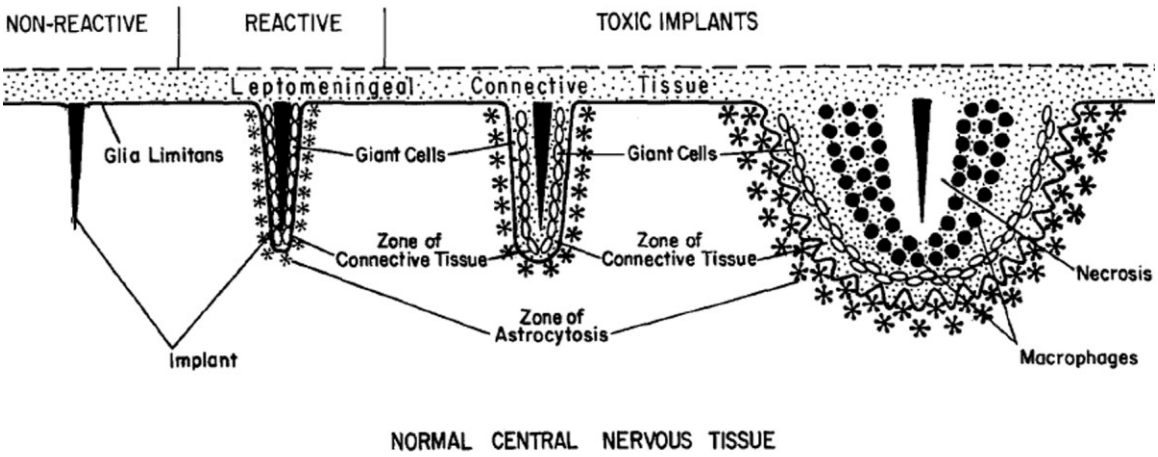



Fig. 2.1: Sketch of immune system response levels, from [71]. The drawing includes astrocytosis regions (asterisks), connective tissue (stippled), giant cells (white circles) and macrophages (black circles).

In order to better understand the sheath development around micromachined probes, Turner, et. al., evaluated tissue responses at four indwelling times up to twelve weeks [72]. The silicon implants each had one 2mm long shank with 16,900μm$^2$ trapezoidal cross-sectional area. Observations made with conventional histology at two and four weeks indicated a continuous yet loosely formed sheath of two to six cell layers which collapsed inward during probe removal. The encapsulation densified over time so that at six and twelve weeks the sheath was compact and did not show signs of shape alteration due to probe removal. Immunohistochemical analysis revealed that the density of GFAP-positive cells (reactive astrocytes) was heightened within hundreds of microns of the probe at the earliest time point (2 weeks), and this radius of intensified activity

actually decreased to tens of microns by the last time mark. Simultaneously, while individual astrocyte processes could be distinguished initially around and within the sheath, later the tissue within the sheath exhibited even stronger GFAP labeling and the cells were so dense that individual ones were difficult or impossible to discriminate.

*In vitro* work by Merrill and Tresco showed that while the electrode impedance rose after coating shanks with cells involved with *in vivo* immune response, the increased impedance was not enough to impede recording [73, 74]. Single-shank silicon probes were implanted in the cortex of rats by Biran, et. al., to further study the foreign body response [75]. The 15µm thick planar devices were 200µm-wide at the base and tapered along the 5mm shank to the tip. As in previous studies, the tissue adjacent to the probe was dominated by activated macrophages, and this area was surrounded with reactive astrocytes. A significant decrease in neuronal density was seen not only within the inflammatory zone but also in the surrounding region. They noted that such findings are not consistent with the theory that electrode recordings diminish over time due to the astrocytic sheath pushing the neurons away from the implant region, since no ring of increased neural density was observed. As an alternative explanation, they propose that the neuronal loss may be due to compounds secreted by the persistent inflammatory response.

Techniques used to stabilize implants in the brain have been considered as possible factors contributing to the immune response. Kim, et. al., investigated the encapsulation of devices with transcranial and intraparenchymal fixation methods [76]. This study used hollow fiber membranes (HFMs) implanted in the brains of adult rats. The transcranially placed devices were anchored to the skull and were in constant contact with the meninges. The intraparenchymally located implants floated in the neural tissue without contact with the meningeal tissue. Immunohistological evaluation revealed significantly greater reaction around the transcranial than the intraparenchymal devices. The proposed factors contributing to this elevated response were the contact with the meningeal tissue and the tethering of the probes. The chronic connection to the meninges may provide a source for meningeal derived fibroblasts which may in turn contribute to the development of a glial/fibroblastic scar around the implant. The fixation of the

device to the skull may cause relative movement of the device within the brain. The distinction in response between these two possible contributors was not unraveled.

Work by Subbaroyan, et. al., approached the issue of tethering forces induced through rotational acceleration of the head by designing a finite-element model of the probe-tissue interface [77]. Calculations revealed increased strains at the tip and sidewalls which appeared to be further exacerbated when coupled with low probe-tissue attachment and stiffer devices. Displacements parallel with the probe axis induced a sheer stress which was maximized near the probe tip. Displacements perpendicular to the probe axis of 1μm resulted in strain regions extending laterally as far as 30μm.

The structure of implanted probes is thought to play a role in the elicited bio-response. Edell, et. al., proposed that blade tips, in sword or chisel shape, which cut though a minimal amount of tissue may be preferable to conical shaped tips which form a band of stretched tissue that remains in tension for the implant duration [78]. Seymour, et. al., explored the role of implant size with polymer probes [79]. The main shank had a cross-section of 70μm by 4μm formed from SU-8 with parylene encapsulation. This structure provided the strength necessary for probe implantation. Extending 100μm laterally from the main shank was a 4μm by 5μm lattice. After a four week indwelling period, the tissue response was found to be greater around the large shank than around the fine open-architecture features.

Perlin developed a series of boron-doped silicon lattice probes to explore the effect of exposed shank area [59]. Five designs, 3mm long, 12μm thick, and 100μm wide ranged from a solid to a mostly open structure with 10μm scaffolds and 25μm support bars; lattice devices with 45μm and 40μm shank widths were also fabricated. In spite of the fine features, these devices were able to penetrate the *pia mater* of guinea pigs. Histological results over several time marks up to twelve weeks from chronic implants in rat cortex indicated neurons were present close to the lattice shanks. Comparisons of the *in vivo* response of one of these lattice designs to a larger solid shank silicon probe by Winslow, et. al., and by Skousen, et. al., showed reduced inflammation [80] and mitigated microglia/macrophage activation and neuronal cell loss [81]. Probes with fold-over back-end tabs (300μm by 200μm) were also made in order to look at the effects of tethering; to date, these have not been chronically implanted.

## 2.2 2-D Structures for Tissue Reaction Studies

Three potentially significant structural factors under the designer's control, which have been hypothesized as playing major roles in eliciting immune reactions to implanted probes, are further considered in this work: the physical volume of the probe shank, the tethering of the probe to the skull, and the cortical surface area covered by the implant. One may naturally expect a larger device to cause a greater response; thus the common assumption is that smaller is better. However, this adage is at odds with the desire to increase the number of electrode sites for an enhanced array-tissue interface, which would not only be useful in neuroscience research but also a prerequisite for many prosthetic applications. The detailed effects of implant volume are therefore worth investigating and may not be as straightforward as initially presumed. Not only may sheer volume be related to immune response, but the arrangement of that volume within three-dimensional space may also play a crucial role. For example, the placement of physical structures may alter diffusion of substances within the neural tissue [82]. Tethering of the probe to the skull may induce shear forces between the probe shank and the surrounding tissue as the brain moves in relation to the skull. This would cause repeated trauma around the implant. Redesign of array structures may allow the probes to "float" in the tissue without direct connection to the skull, eliminating the tethering issues. Such a design could rely on resting the array platform or handling tab on the cortical surface. However, occluded cortical surface area might also cause changes in the immune response.

### 2.2.1 Shank Design

In order to investigate these key issues involved in electrode array biocompatibility, probes and other structures were developed which varied critical parameters. The first design parameter considered was shank volume. When using probe technology with boron etch-stops to define implant thickness, the two-dimensional layout becomes the main specification through which volume can be regulated. To facilitate a comparison between probes with a specified outline and variation in enclosed volume, a suite of fourteen two-dimensional single-shank probes was designed as shown in Fig. 2.2. The largest volume structure consisted of a 3000μm long and 300μm wide solid shank,

excluding the tip and back-end regions. Although the width of this probe was significantly larger than that of typical shanks, a design with such a substantial footprint was chosen in order to cover a wide spectrum of enclosed volume, as enumerated in Table 2.1. The tip angle is $20^{o}$ for ease of insertion. The rectangular portion of the probe back-end is 600µm by 1150µm which then tapers to the shank width over a distance of 300µm. The open-architecture layouts had the same external dimensions but variations in their internal structural supports. The main considerations for lattice designs are the required shank strength for penetrating the *pia mater* during insertion and preserving sufficient space on the shank surface for the interconnect lead lines and electrode sites. In view of this, selected lattice configurations with block, brick, picket, and truss supports and rib widths of 15, 10, and 5µm were developed.

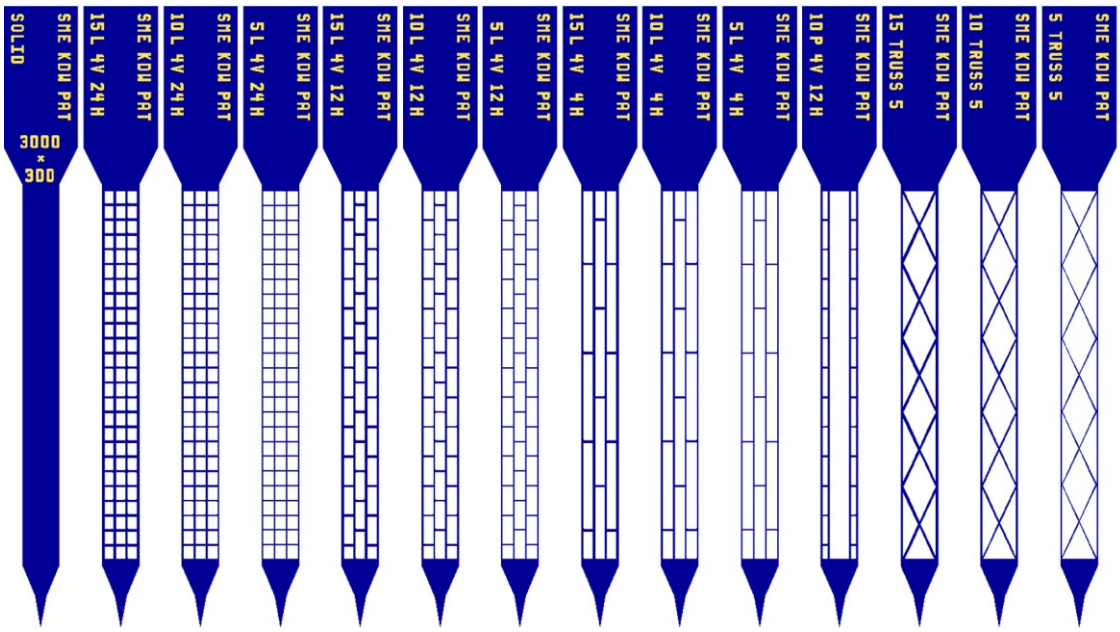



Fig. 2.2: Layout of solid and lattice probe designs (solid, block, brick, picket, and truss) using the standard back-end for the tethered setup. Probes have rib layout widths of 15, 10, and 5µm.

**Table 2.1: Shank Layout Area**

| Solid | Rib | Block-24H | Brick-12H | Brick-4H | Picket-12H | Truss-5 |
|---|---|---|---|---|---|---|
| $0.900mm^2$ | **15µm** | $0.273mm^2$ | $0.227mm^2$ | $0.196mm^2$ | | $0.184mm^2$ |
| | **10µm** | $0.189mm^2$ | $0.155mm^2$ | $0.132mm^2$ | $0.134mm^2$ | $0.125mm^2$ |
| | **5µm** | $0.100mm^2$ | $0.080mm^2$ | $0.067mm^2$ | | $0.064mm^2$ |

### 2.2.2 Stabilization Options

The second factor considered was the method of probe stabilization. Some implants are secured to the skull at the back-end. This causes potential tethering issues as the brain moves in relation to the skull but the probe is unable to fully move with it. An alternative to this implantation technique is to disconnect the probe from the skull so that it can float in the neural tissue. Two back-end designs were utilized to explore this issue. The first design, already introduced above, consists of a probe shank and back-end of one solid piece of boron-doped silicon. This allows for easy handling of the probe and fixing of the implant to the skull in a tethered setup. The second design employs a tab as a separate piece of silicon from the probe shank but connected to it with a foldable layer of 4μm thick electroplated gold. The 600μm by 500μm tab is intended for handling purposes. Six bendable beams per probe, 50μm wide at 100μm pitch, extend 50μm past each side of the 100μm gap between the shank back-end and tab. During probe preparation, the tab is folded at an approximately ninety degree angle and secured with medical grade silicone (silastic) or other material. Using this back-end, the probe shank can be implanted in the neural tissue with the tab placed on the cortical surface. The *dura* can be replaced, and the low profile of the folded tab ensures that contact with the skull is not made. Two designs, one solid and one perforated, were used for the tabs; eight probe shank designs were coupled with these two tab designs as shown in Fig. 2.3.

### 2.2.3 Cortical Surface Devices

The third aspect taken into account was the area of the cortical surface on which the implant rests. Although this is a consideration with the fold-over tabs in the non-tethered probe design, it is even more a matter of consequence with three-dimensional arrays which incorporate a relatively large platform perpendicular to the probes. In addition to using a small footprint for the handling tab of the non-tethered probes, this issue was taken into account by fabricating probes with both solid and lattice tabs as described above. For investigation into the particular issue of covered cortical surface area, stand-alone tabs/platforms were also fabricated. Two outer dimensions were used, 600μm by 500μm and 1200μm by 1200μm; each had a solid option as well as one or two lattice configurations as illustrated in Fig. 2.4.

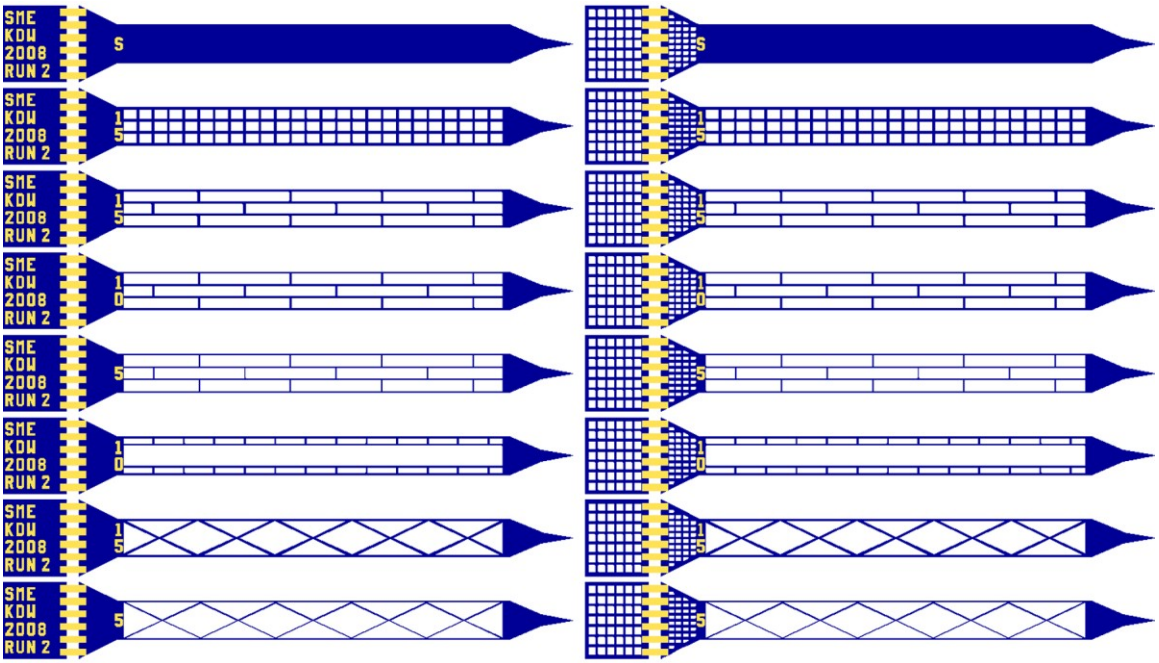



Fig. 2.3: Layouts of lattice probe designs using solid and perforated fold-over tabs for the non-tethered setup.

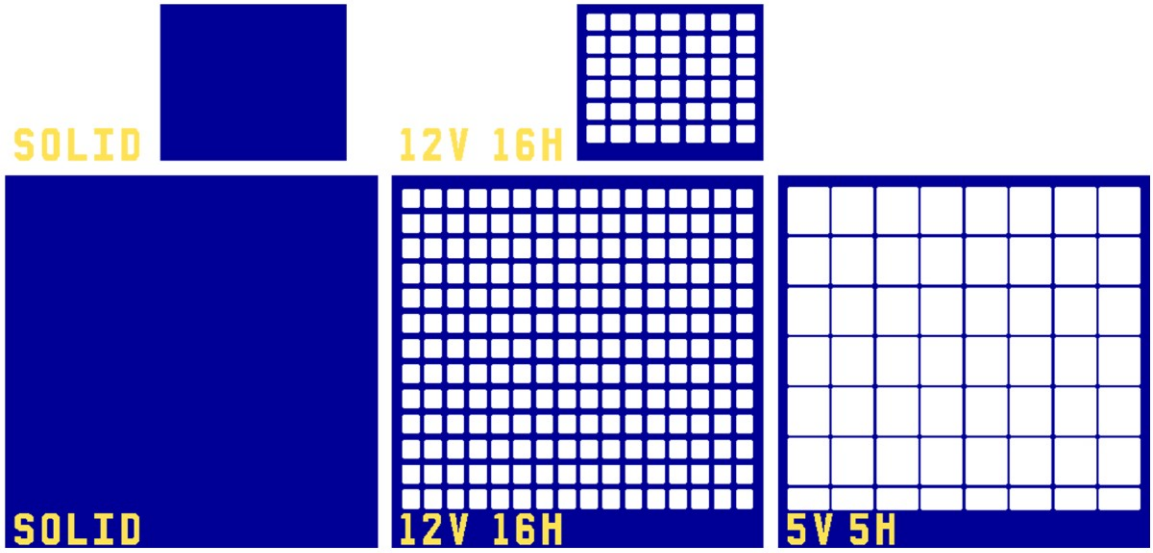



Fig. 2.4: Layout of stand-alone platforms to study effects of occluded cortical surface area. The smaller version has a footprint of 600µm by 500µm and the larger one is 1200µm by 1200µm. The widths of the vertical and horizontal supports are indicated in the image for each design.

## 2.3 Fabricated Devices

The histological bio-response studies presented here do not incorporate neural recording or stimulation. Therefore, a simplified process flow was used to fabricate the lattice devices, shown in Fig. 2.5 through Fig. 2.9, which did not include electrode sites or interconnects. A boron etch-stop is used to set the substrate thickness at approximately 12μm. In order to simplify the masks, blanket boron at the wafer- or region- (to allow folding tabs) level was implemented. An oxide-nitride-oxide dielectric stack (1500Å/3000Å/1500Å) was included followed by the electroplated gold beams (~4μm) for tab folding. After the dielectric stack was etched, deep reactive ion etching (DRIE) was employed to etch through the diffused boron to finish defining the probe shape. The wafers were thinned from the back-side and then released in a wet EDP (ethylene diamine, pyrocatechol, and water) etch. Since blanket boron and DRIE define the probe, the sharp tips have a chisel shape.

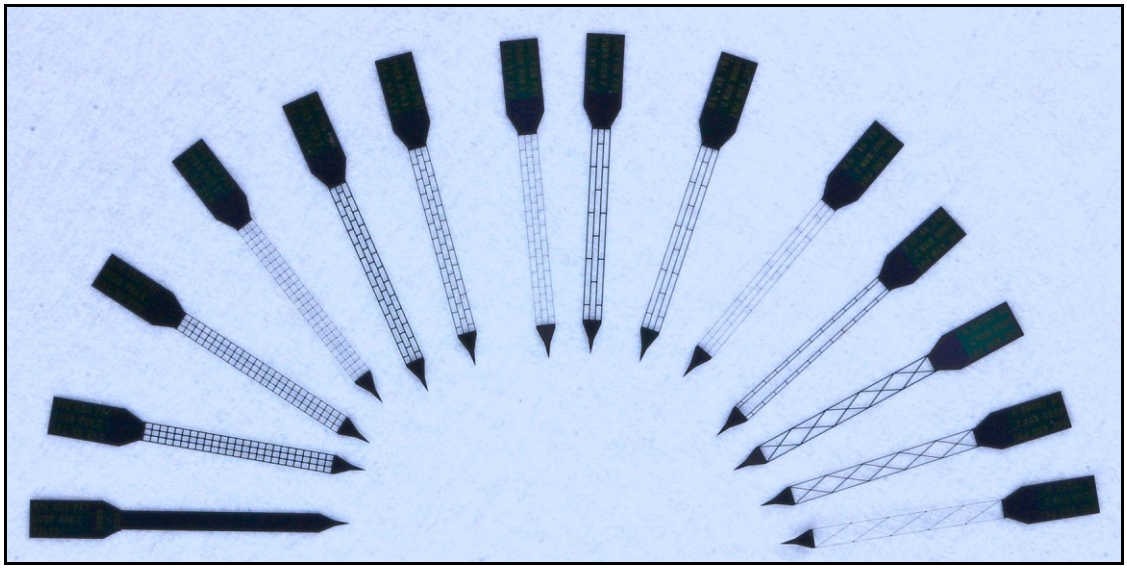


Fig. 2.5: Photograph of 2-D bio-response probes with fourteen shank designs.

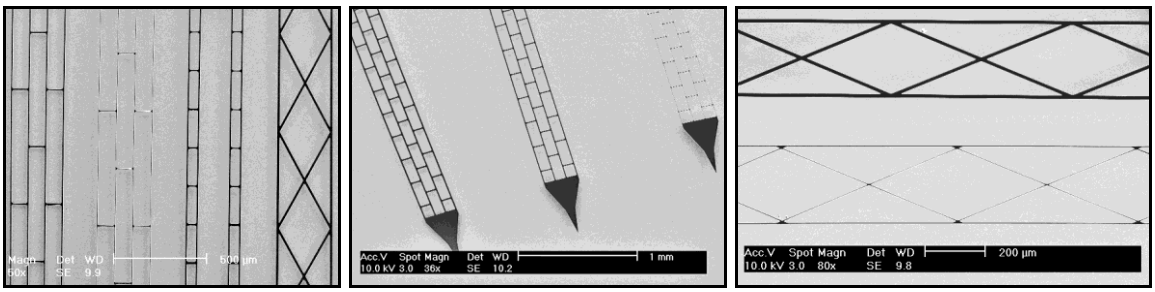



Fig. 2.6: SEM images of 2-D bio-response probes with rib widths of 15, 10, and 5μm.

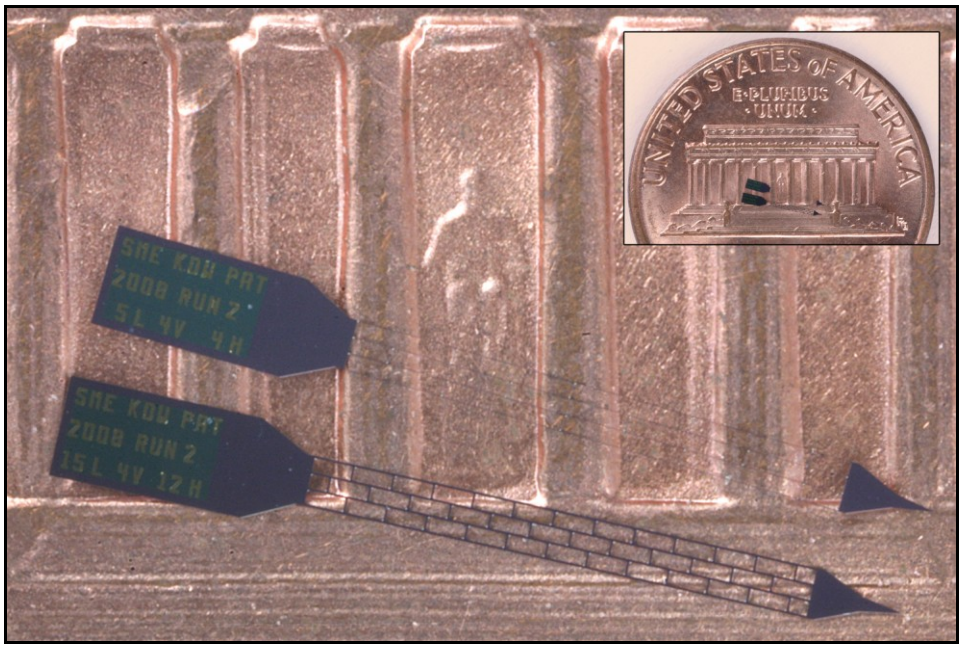



Fig. 2.7: Probes with 15µm and 5µm ribs in brick design on the back of a U.S. penny.

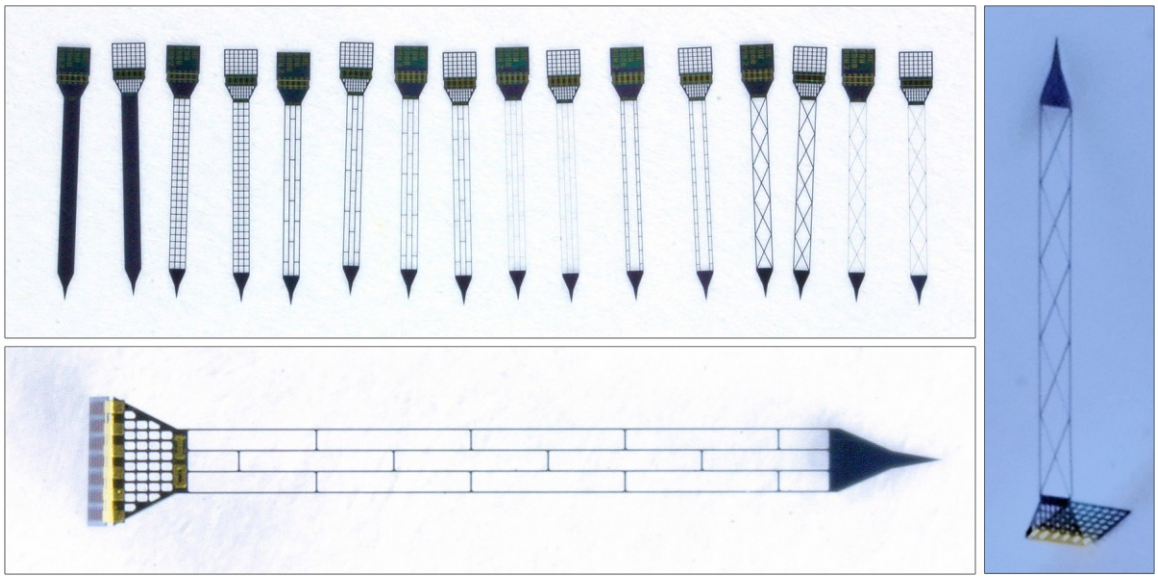


Fig. 2.8: Photographs of bio-response probes with tabs for the non-tethered setup.

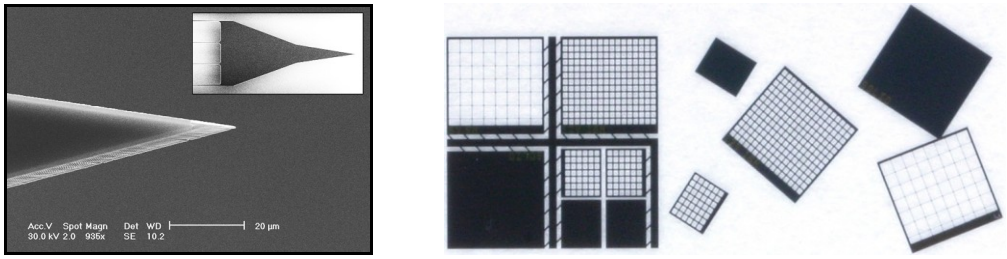



Fig. 2.9: SEMs of a chisel shape probe tip (left) and photograph of cortical structures fabricated with and without snap-out tabs (right).

## 2.4 *In Vivo* Results with 2-D Lattice Probes

Over four hundred released 2-D devices were shipped to collaborators for bio-response related experimentation. In preparation for insertion, the *dura mater* is removed; implantation trials verified that the solid and picket probes, among others, could successfully be inserted through the *pia mater* without fracturing.

### 2.4.1 Histology & Immunostaining

Histology, the study of cells through the use of tissue slices, is one of the main techniques employed in understanding the elicited immune system reaction to an implanted device. At the conclusion the *in vivo* studies of this work, sections were batch stained, imaged at same exposure, and light field corrected for tissue response comparison. The stains used are enumerated in Table 2.2.

**Table 2.2: Immunostaining Materials***

| Stain | Target | Type | Maker | Item # | Conc |
|---|---|---|---|---|---|
| CD68 ED-1 (green) | Activated microglia or macrophages | 1° ms IgG1 | Serotec | MCA 341R | 1:1000 |
| | | 2° A 488 gt x ms IgG1 | Molecular Probes | A21121 | 1:500 |
| IgG (red) | Immuno-globulin Gamma | 1° BIOT gt x rt IgG | Southern Biotec | 3050-08 | 1:500 |
| | | 2° A594 strep | Molecular Probes | s11223 | 1:500 |
| NeuN (green) | Neuronal Nuclei | 1° ms IgG1 | Chemicon | MAB377 | 1:1000 |
| | | 2° A 488 gt x ms IgG1 | Molecular Probes | A21121 | 1:500 |
| GFAP (red) | Astrocytes | 1° Rb IgG | DAKO | Z0334 | 1:1000 |
| | | 2° A594 Gt x rb IgG | Molecular Probes | A11037 | 1:500 |
| MOSP⌖ (green) | myelin/ oligodendrocyte specific protein | 1° ms IgM | Chemicon | MAB 328 | 1:1000 |
| | | 2° A 488 gt x ms IgM | Molecular Probes | A21042 | 1:500 |
| NF200 (red) | Neuro-filament | 1° Rb IgG | Sigma | N5264 | 1:1000 |
| | | 2° A594 Gt x rb IgG | Molecular Probes | A11037 | 1:500 |
| Sections counterstained with DAPI (blue) to identify cell nuclei. | | | | | |
| All stains diluted in block: 4% (v/v) normal goat serum, 0.3% (v/v) Triton-X-100, and 0.1% (w/v) sodium azide in 1x PBS. | | | | | |
| 1° Stain is the antibody that binds to the antigen of interest.<br>2° Stain is the fluorescently labeled antibody that binds to all antibodies of a certain isotype from a given species of animal.<br>⌖ For the MOSP stain, the 1° antibody is bitotin functionalized and the 2° stain is a labeled sterpavidin that binds to the biotin. | | | | | |
| * Table courtesy of Mr. John Skousen, University of Utah. | | | | | |

### 2.4.2 2-D Bio-response Pilot Study

A pilot study was conducted in which two cohorts of probes were stereotactically implanted for eight weeks in rats [83]. The implantation was done through the cortex into CA1 in the right hemisphere, 2.0mm lateral to and -3.2mm of Bregma, and 3mm deep. The device position was secured with custom polyurethane grommet. The selected shank designs were the 300µm wide solid shank (N=5) and 15µm rib lattice shank (block-15L-4V-24H) with the same footprint (N=6). A scanning electron microscope image in Fig. 2.10 shows the structural difference between the two shank designs.

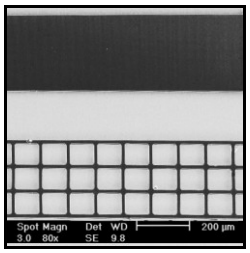



Fig. 2.10: SEM of the solid and 15µm rib block for the eight week pilot *in vivo* study.

Upon conclusion of the eight-week implant duration, histology and immunostaining were performed as described in 2.4.1. Previous work has shown that cellular processes tend to intertwine with lattice structures [81]. While this is advantageous for probe stabilization, probe explantation for investigation of the bio-response causes removal of tissue along with the device. In this study it was possible to section through the lattice probe, thus maintaining intact the probe-tissue interface. The sectioning required removal of the solid shank. Although the sample size was small, preliminary observations encouraged further studies.

A horizontal section from each cohort is visually compared in Fig. 2.11 with staining for DAPI, IgG, and ED-1 (CD68). The tissue interface around the solid shank is circumscribed with a broad oval in which there appear less cell nuclei (DAPI) than in the tissue far from the implant. The border of the oval itself is higher in density of both cell nuclei and activated microglia/macrophages (ED-1) than the surrounding tissue. There is a notable distinction between the shape of this immunoreactivity and that of the lattice device. Whereas the solid implant elicits an ovalescent response, that due to the lattice implant remains more closely confined to the implant site. Thus, there is less visible disruption in the surrounding tissue with the lattice shank.

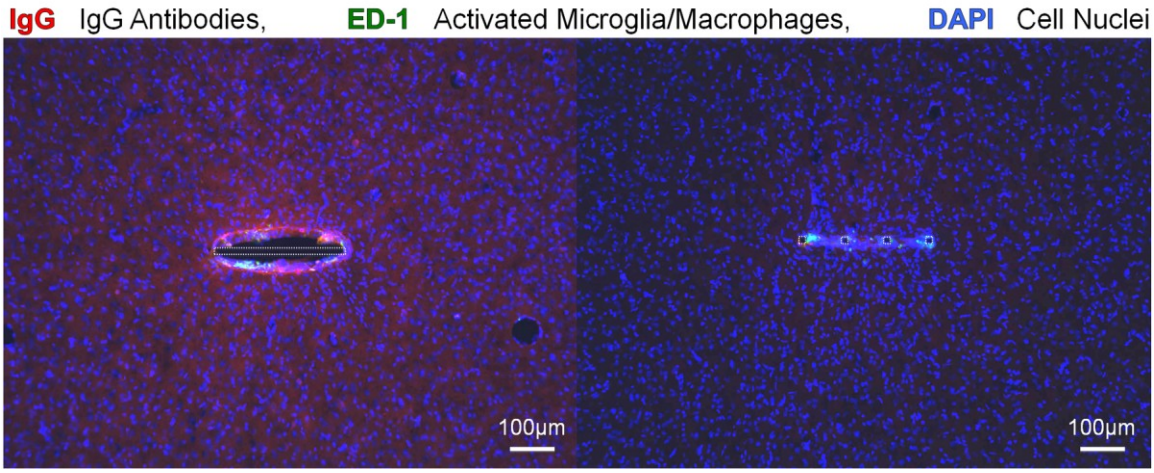



Fig. 2.11: Horizontal sections from the solid (left) and lattice (right) pilot study implants showing stains for IgG, ED-1, and DAPI [84]. Dashed shapes indicate probe position.

Photographs are presented in Fig. 2.12 of horizontal sections with NeuN, IgG, ED-1 and GFAP staining. With the staining for neuronal nuclei the oval-shaped response is again apparent around the solid probe; however, "NeuN positive cells are found adjacent to the lattice probe" and the "tissue integrates into the lattice probe and in some cases viable neurons are very close to structures" [85]. The IgG staining reveals a more heightened response throughout the surrounding region with the solid implant as compared to that with the lattice device. This indicates issues in the blood brain barrier as IgG is normally found only within the vasculature. It may also be noted that the "distance from electrode face to end of ED-1 positive zone [is] great[er] on solid vs. lattice probe. Lattice probe ED-1 staining localized more to the lattice window" [85]. It is hypothesized that the immune reaction is not only due to the cross-sectional area but also to the distribution of that area since this affects diffusion of soluble factors [85]. As such, not only rib size but also rib spacing would play a role in the intensity of the response. This would accordingly be a critical consideration in the design of multi-shank 2-D probes and multi-probe 3-D arrays in determining shank and probe pitch. The aforementioned role of the diffusion of soluble factors may also be one of the reasons why the "GFAP response appears altered surrounding lattice probes" [85]. In summary, the immune response to the lattice structure exhibited a reduced amount of activated microglia/macrophages and less neuronal cell death than the solid device with the same footprint [83].

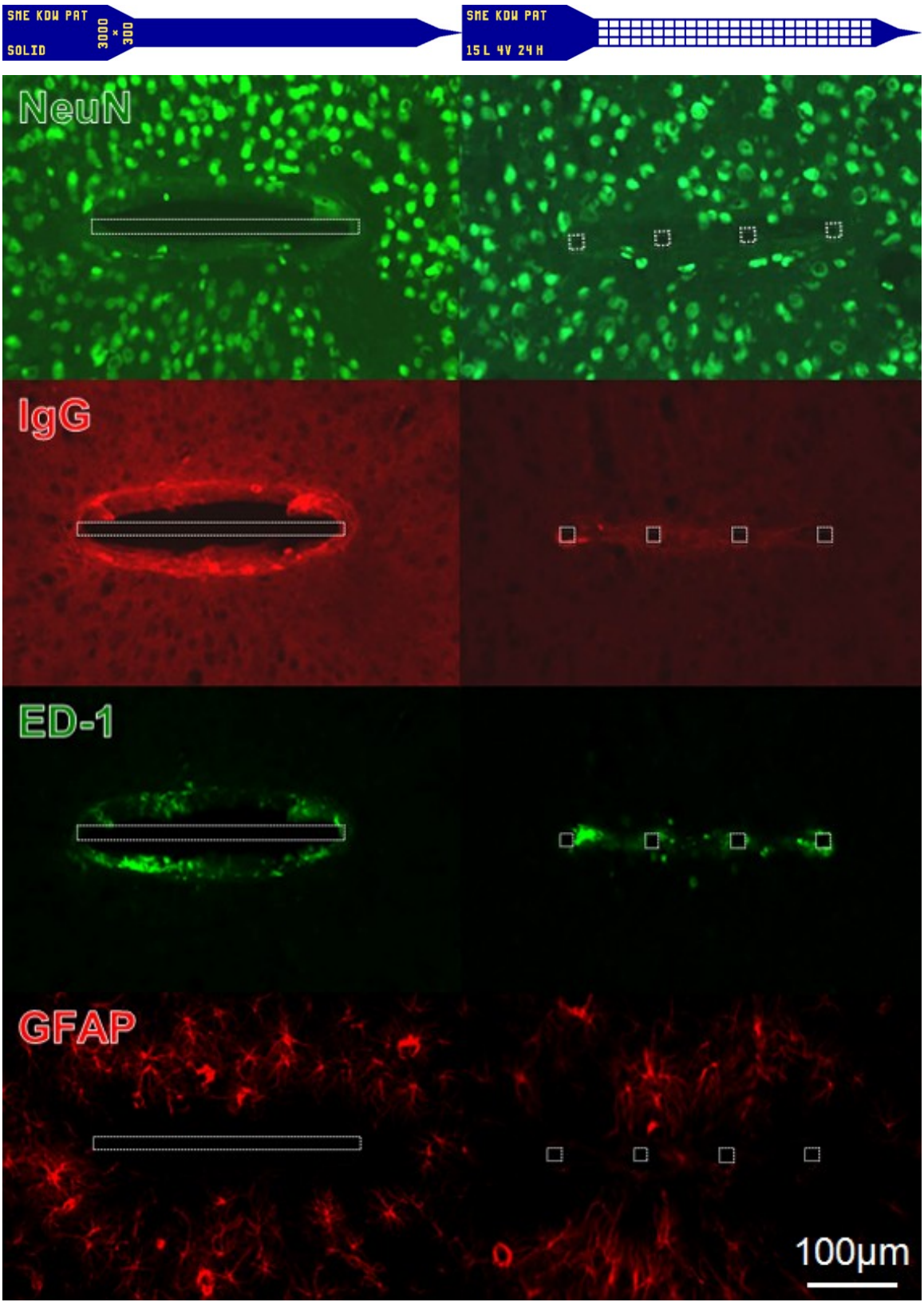



Fig. 2.12: Horizontal sections (perpendicular to the long shank axis) from the solid (left) and lattice (right) pilot implants [84]. Dashes indicate probe position.

### 2.4.3 2-D Probe Quantitative Data Analysis *In Vivo* Study

Understanding the brain tissue response at the biotic-abiotic interface enables technology developments for further mitigating undesirable immune system reactions. Quantitative immunohistochemical analysis was performed in order to obtain a numerical comparison between the foreign body response in levels 3-6 of the cortex due to the implanted solid (N=4) and lattice (N=5) probes. This data analysis employed horizontal sections, perpendicular to the implantation tract, from the 8 week *in vivo* experiment. Whereas the pilot study simply presented single tissue sections from selected animals, the quantitative study used multiple sections per animal which were batched stained, light field corrected, and then averaged. After determining the mean response for each biomarker on an animal by animal basis, the responses were combined within the two cohorts to determine the results for each probe type. Multiple sections per animal are required for statistical significance and group staining is essential to reduce extraneous variability due to the stain preparation. The response to the lattice probes was significantly less than that to the solid devices. Representative horizontal sections for the DAPI, ED-1 (CD68), IgG, GFAP, and NeuN stains are shown in Fig. 2.13 and Fig. 2.14 after image adjustment by background subtraction of primary controls.

While other studies have shown an inverse correlation between the presence of inflammatory cells and recording capability [86], this relationship is yet to be fully understood. However, it is known that macrophage secreted factors modulate the tissue reaction to implanted devices [81, 87]. Quantitative data for the ED-1 response in this work, assessing activated microglia/macrophages, are shown in Fig. 2.15. The line profile graph represents the average fluorescent intensity of the stain (bold line) as a function of the distance from the center of the probe; the shaded portion indicates the standard deviation. The immunostain graph for the solid device goes to zero within the device boundary since cells can not enter the structure; however, cells are able to intertwine with the lattice architecture. The average peak ED-1 immunoreactivity for the lattice device was only 50% of that for the solid shank. The bar graph shows the area under the curve (AUC) of fluorescent intensity in 50μm steps; this is technically a volume measurement since the tissue sections are each 30μm thick. Within the first and second 50μm bin, the average ED-1 response for the lattice device was 40.8% and 15.8%

of that for the solid shank, respectively. The differences between the ED-1 responses of the solid and lattice structures within these two bins are statistically significant ($p<0.05$) signifying reduced persistent inflammation with the lattice device.

Graphs for the IgG response, appraising the dysfunction of the blood-brain barrier, are shown in Fig. 2.16. The line profile shows a substantial difference between the two devices and the IgG immunoreactivity for the lattice probe within the first 50µm bin was merely 14% of that for the solid probe. The differences between IgG bio-response to the two structures are statistically significant ($p<0.05$) for the first five bins.

Quantitative results for the GFAP immunoreactivity, evaluating the presence of reactive astrocytes, are shown in Fig. 2.17. While astrocytic hypertrophy is seen in both cases, there is no statistically significant difference between the reactivity for the solid and lattice architectures. Notably, some studies have not found a correlation between GFAP and neuronal density, but have shown a correlation between ED-1 and NeuN [88].

A quantitative graph for the mean NeuN density, assessing the presence of neurons, is presented in Fig. 2.18. Within the first 50µm, there was an extreme increase in the chronic neuronal survival for the lattice probe (87%) over the solid device (36%) as a percentage of normal NeuN density, where the normal density is defined as that of the background NeuN density 400-500µm away from the implanted device. The difference in NeuN density between the two structures in the first bin is statistically significant ($p<0.05$). Making the considerable assumption that the neuronal density along the entire length of the implant is the same as the average neuronal density in layers 4-6 of the cortex, it can be hypothesized that the lattice device saves 1900 neurons within the first 50µm bin (laterally). This finding is of considerable value since the first bin overlaps with the primary recording range of electrode sites.

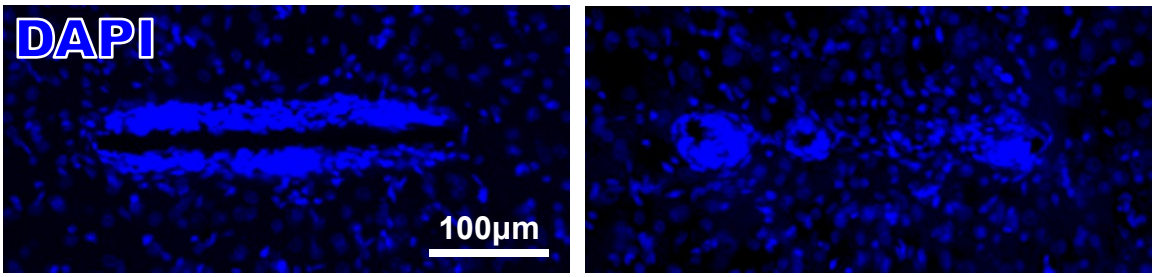



Fig. 2.13: Horizontal DAPI sections (perpendicular to the long shank axis) from the solid (left) and lattice (right) quantitative study probe implants [84].

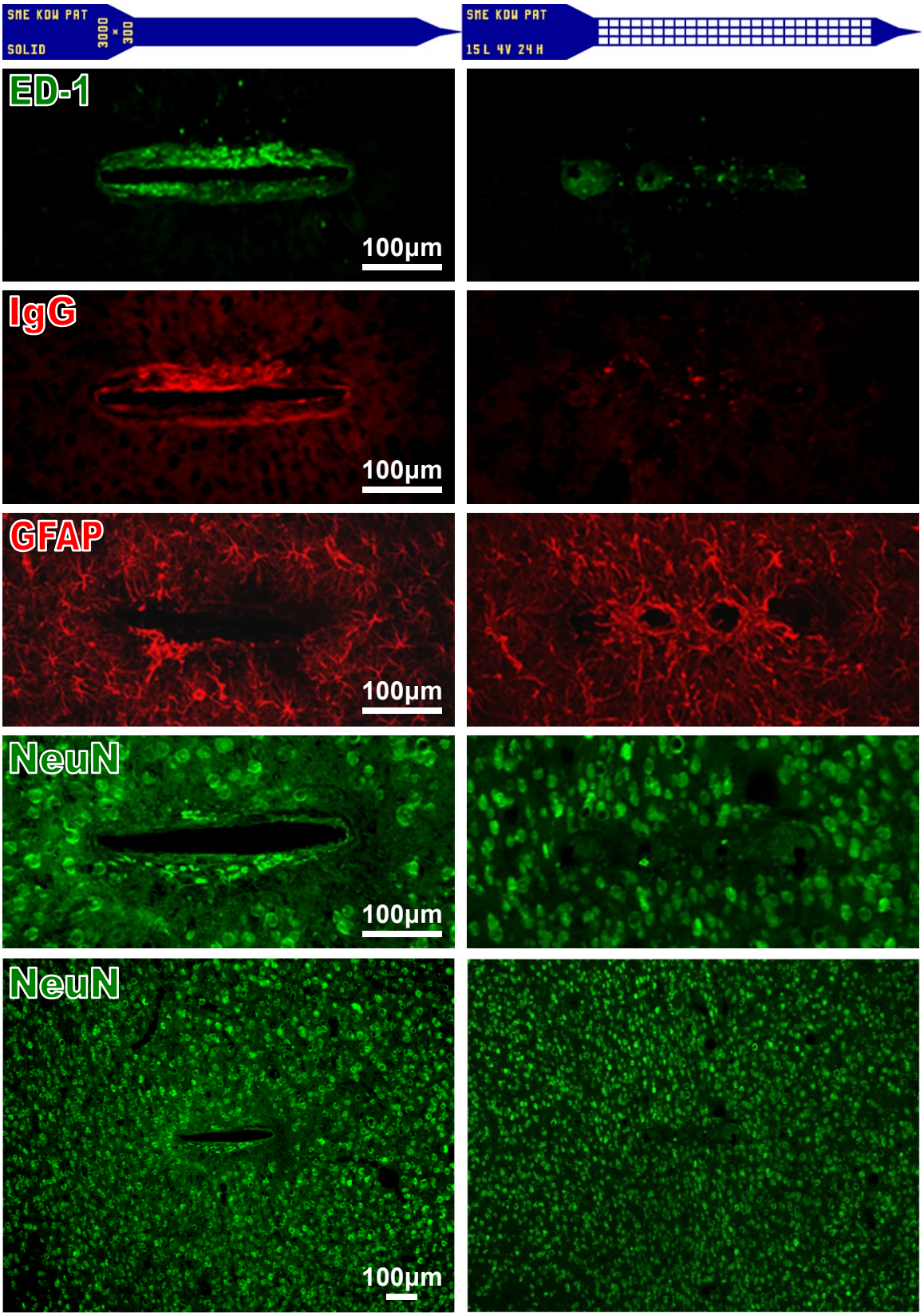



Fig. 2.14: Horizontal sections (perpendicular to the long shank axis) from the solid (left) and lattice (right) quantitative study probe implants [84].

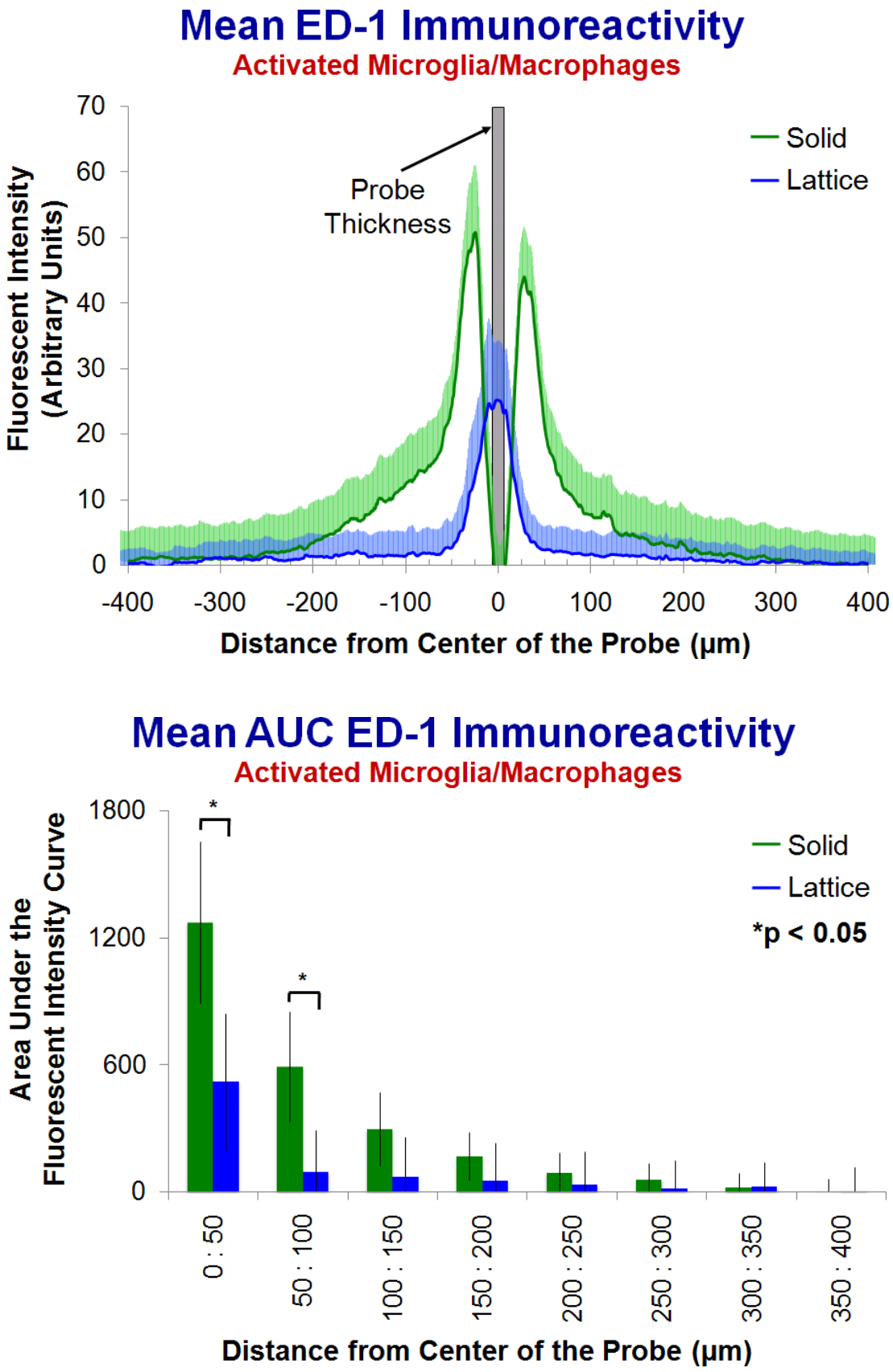



Fig. 2.15: Quantitative data of the ED-1 immunostain distribution [84].

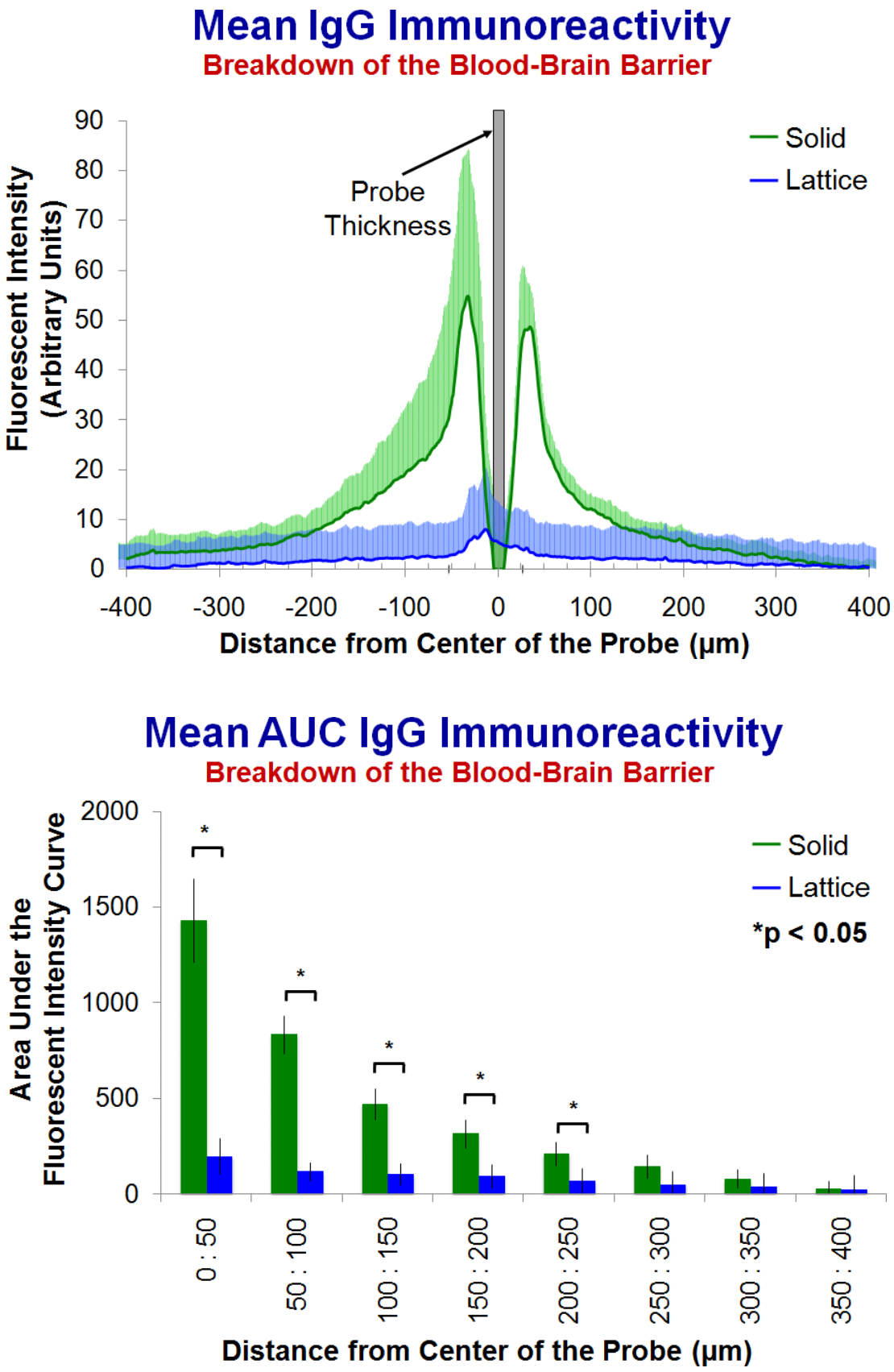



Fig. 2.16: Quantitative data of the IgG immunostain distribution [84].

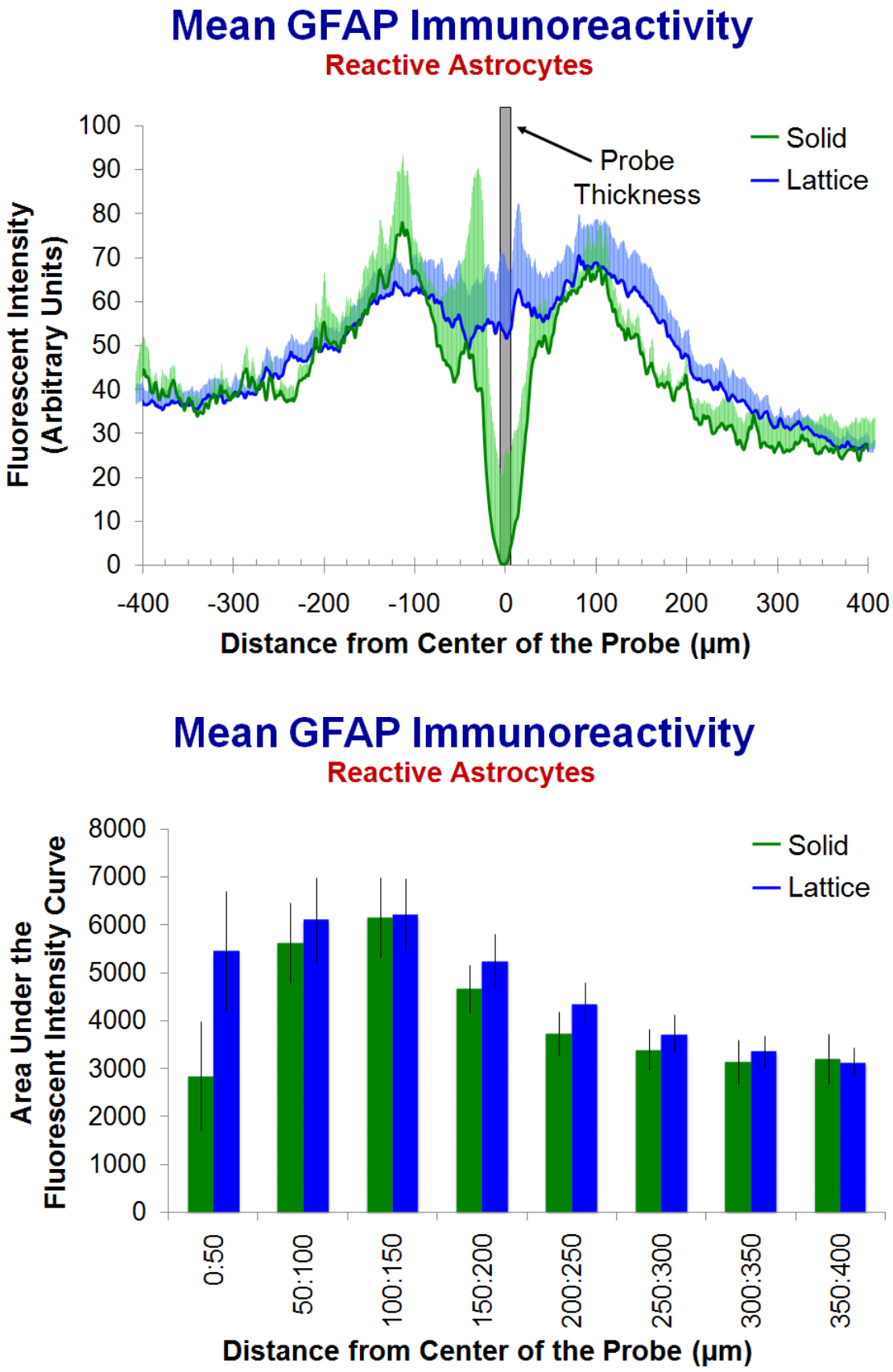



Fig. 2.17: Quantitative data of the GFAP immunostain distribution [84].

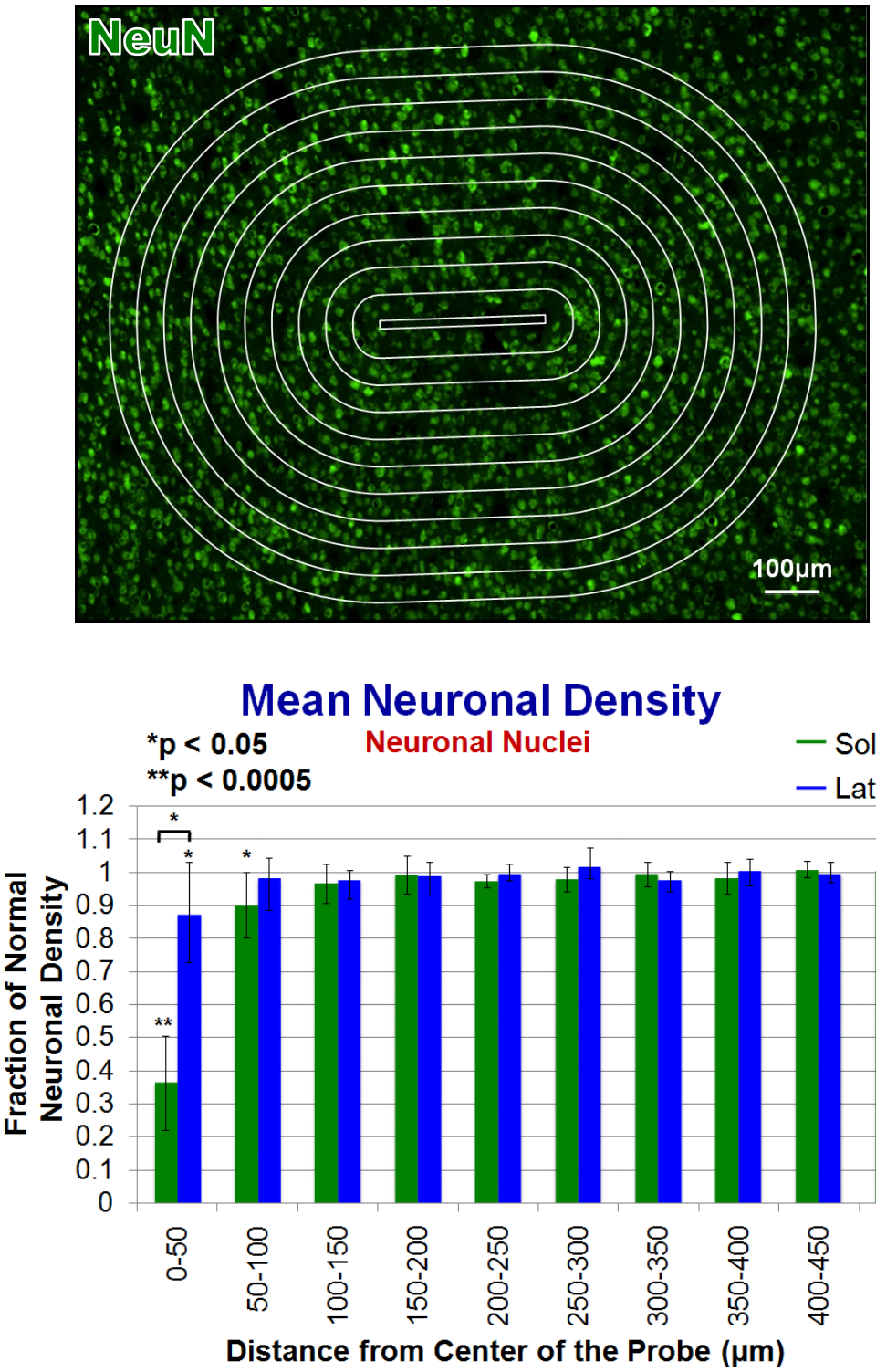



Fig. 2.18: Horizontal section with overlay of the 50µm bins (top) and quantitative data of the NeuN biomarker distribution (bottom) [84]. The first bin shows a statistically significant difference ($p<0.05$) in NeuN density between the solid and lattice architecture with a substantial increase in the chronic neuronal survival for the lattice probe (87%) over the solid device (36%) as a percentage of background (400-500µm bins) NeuN density.

## 2.5 Surface Coatings

While the surface of the probes (standard boron-doped silicon back-side covered with thin native oxide and LPCVD deposited oxide front-side) is not considered to be neurotoxic, it does not inherently promote neural growth or encourage the attachment of neural processes. The use of coatings to modify the surface of the devices to which the biological host is exposed has the potential to be a relatively simple yet effective means by which to modulate the response of both the immune system and the targeted cell type.

Some work has already been done in this field, such as the study by Shain, et. al., [89]. Peripheral injections of dexamethasone attenuated the density of glial fibrillary acidic protein (GFAP) positive cells (astrocytic response) surrounding silicon micromachined penetrating probes. Control and dexamethasone ribbons inserted in the brain were then analyzed; the drug-containing ribbon had a significantly lower immune reaction than the control. This indicates implanted medications which release over time may be a means, while the implanted amount lasts, of providing localized intervention.

In another study, by He, et. al., 5mm-long, 15μm-thick boron-doped silicon substrate probes with a shank width of 200μm tapering to 33μm were coated with eight bilayers of Polyethyleneimine (PEI) and Laminin-1 (LN) and implanted in the cortex of rats for up to four weeks [90]. At the one week mark, a decrease in neuronal nuclei density was found in both coated and uncoated controls up to 30μm from the device. Also at one week, similar ED-1 (activated microglia/macrophages) and GFAP (astrocytes) expression was observed between the coated and uncoated probes. At four weeks, the coated device had reduced ED-1 and GFAP intensity compared to the control.

Two coating methodologies were developed for use with the devices presented here [81]. The first scheme makes use of an alginate hydrogel and the second of a HPMA polymer hydrogel as illustrated in Fig. 2.19. Both methodologies invoke covalent tethering to the oxide on the probe surface and provide options for functionalizing with biomolecules such as Laminin and $NH_2$. With these schemes applied to the open-architecture devices, the advantage of coating, namely surface modification, and an advantage of the lattice structure, that of allowing diffusion of soluble factors within the probe footprint, are combined. The coating procedures were explored with eight shank designs. Four designs (solid, block-15L, brick-15L-12H, truss-15L) went through the

entire process successfully; two designs (brick-5L-12H, brick-5L-4H) broke when vacuum was applied in the oxygen plasma chamber and two (picket-10, truss-5L) broke due to the force exerted on the probe by the gel as it contracted during the drying phase. Fig. 2.20 and Fig. 2.21 present photographs of coated lattice probes. The gel thickness can be in the micron to nanometer range as shown in Fig. 2.22 and Fig. 2.23 [88].

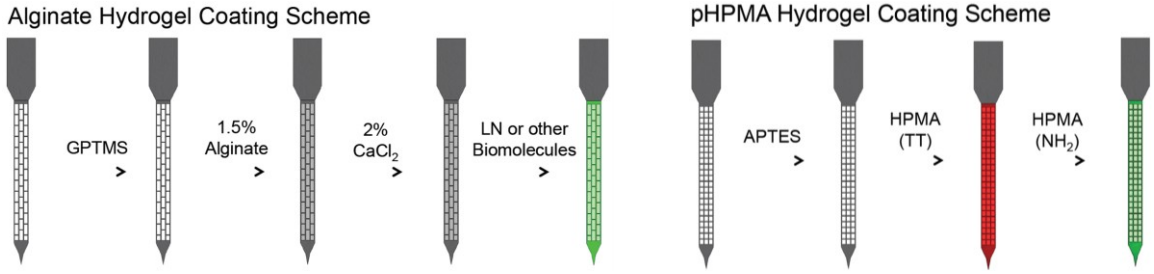



Fig. 2.19: Alginate (left) and HPMA (right) coating schemes [84]. For both, first a dry oxide growth and oxygen-plasma clean was performed. For the alginate scheme, 3-gylcidoxypropyltrimethoxy silane (GPTMS) was coupled to the $SiO_2$ probe surface by chemical vapor deposition (CVD). A sodium alginate/$H_2O$ solution was used to tether the alginate hydrogel; gelation was accomplished in a $CaCl_2/H_2O$ solution. The exposed surface was further functionalized with biomolecules including Laminin (LN). For the second scheme, aminopropyltriethoxy silane (APTES) was coupled to the $SiO_2$ surface which was then reacted with N-(2-hydroxypropyl)methacrylamide (HPMA polymer) containing reactive ester thiazolidine-2-thione (TT) and a TexasRed label. Remaining TT was reacted with another HPMA polymer containing $NH_2$ terminated and FITC labeled side chains.

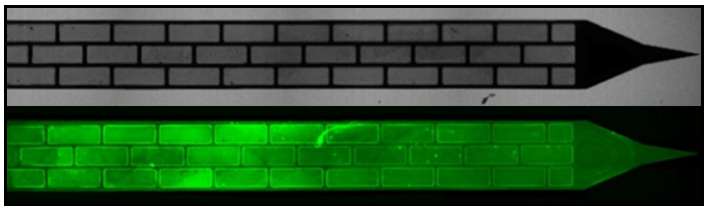


Fig. 2.20: Brightfield and fluorescent images of lattice probes with tethered alginate (top) and subsequently functionalized with Laminin (bottom) [84].

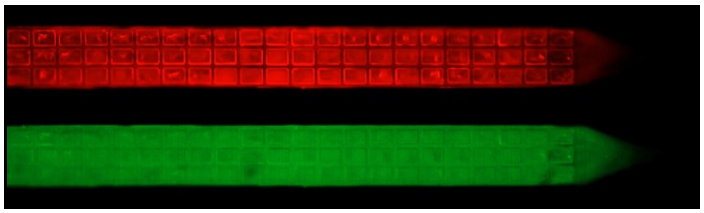


Fig. 2.21: Fluorescent images of coated lattice probes with tethered HPMA polymer functionalized with TexasRed labeled TT (top) and after further functionalization with FITC labeled $NH_2$ (bottom) [84].

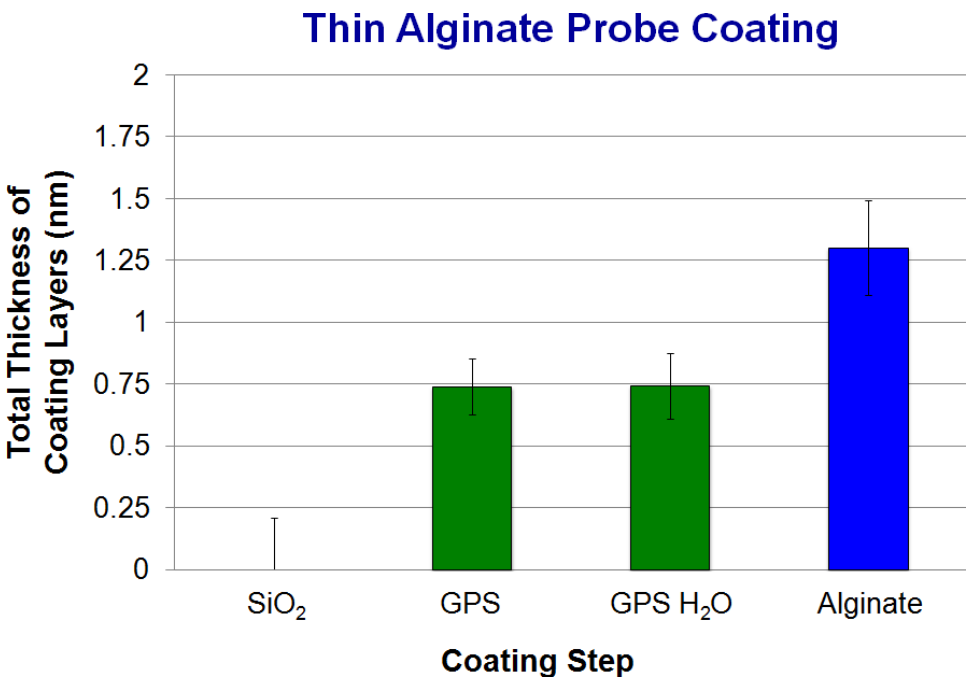



Fig. 2.22: Step-by-step measured gel thickness for the alginate coating scheme [84]. The significant increase in coating thickness from the oxide growth to the GPS step indicates coupling occurred. The GPS $H_2O$ bar acts as a negative control and shows that mere exposure to water does not substantially change the GPS thickness, whereas moving from the GPS to the alginate tethering step there is again a significant increase in film thickness.

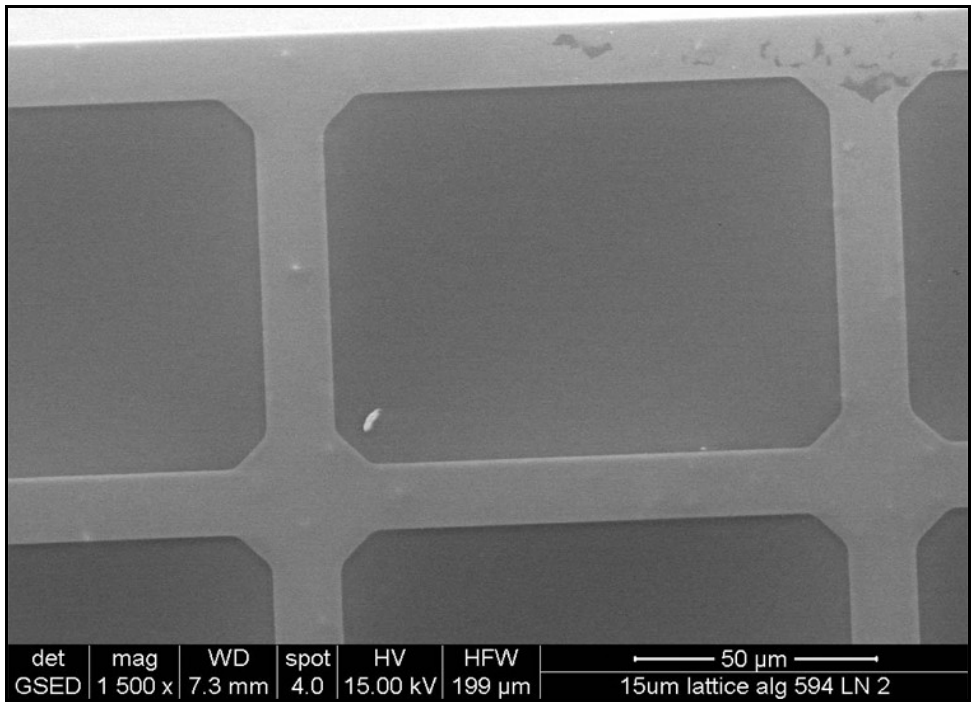



Fig. 2.23: Environmental SEM image of a 15µm-ribbed lattice probe with thin Laminin-functionalized alginate hydrogel coating [84].

## 2.6 Development of 3-D Lattice Arrays

While studies with single-shank 2-D probes enable research to concentrate on particular aspects of the biocompatibility question in a narrow environment, expansion to multi-shank 2-D probes and 3-D arrays provides a more complete picture of the overall bio-response setting. This is particularly important for chronic neural mapping and prosthetic applications in which a high site density requires the support of multiple shanks arranged in 3-D space. In order to support such investigations, 3-D arrays have been developed. These devices may be categorized by their shank width (wide or narrow) or by their 3-D probe to probe alignment (parallel only or parallel and perpendicular).

### 2.6.1 3-D Structure

The silicon block platform methodology was employed for the three-dimensional structure of the lattice arrays [59]. The approximately 500μm thick silicon platform performs mechanical stabilization of the 2-D multi-shank probes. Since these studies do not make use of the electrode sites, dummy probes without lead lines or sites were fabricated. The thickness of the probe back-end is thus the same as that of the probe shanks (approximately 13μm including the dielectric stack). The 300μm deep top platform slots were designed with a 4μm thickness tolerance which results in a 17μm-wide slot. The 200μm-deep bottom slots are 19μm wide, giving a 1μm alignment tolerance in each direction. Concurrently with the slot etches, rim etches are performed to release the platform from the wafer. The top and bottom rim etches are 17μm and 16μm-wide respectively. The slots form a ledge within the platform upon which the probes rest so that once inserted they are countersunk in the platform forming a low-profile device. The top of the platform is sealed with medical-grade silicone or other material to secure the probes.

### 2.6.2 Exclusively Parallel Probe Arrays

The most straightforward approach to three-dimensional arrays is to place identical two-dimensional probes in parallel. This is the methodology employed with the exclusively parallel probe design. The 3mm by 2.2mm block platform includes eleven probe slots at a pitch of 200μm, providing a base for flexibility in the number of probes

and their spacings, which can both be determined at the time of assembly. Wide- and narrow-shank probes are available for this platform; both designs have the same back-end dimensions. Fig. 2.24 illustrates the platform and probe back-end. The shanks for the wide shank probes are identical to those described for the 2-D probes above. However, each probe has three shanks. Probes were fabricated with 200, 400, and 800µm shank spacings (gap) as shown in Fig. 2.25.

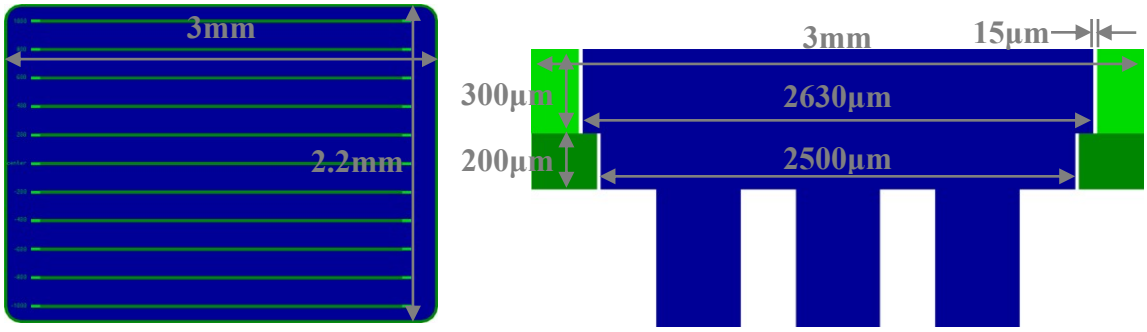



Fig. 2.24: Top view of the parallel-probe platform (left) and cross-sectional drawing of a probe in a platform slot (right). The light and dark green indicate the top and bottom slot etches respectively of the full thickness wafer.

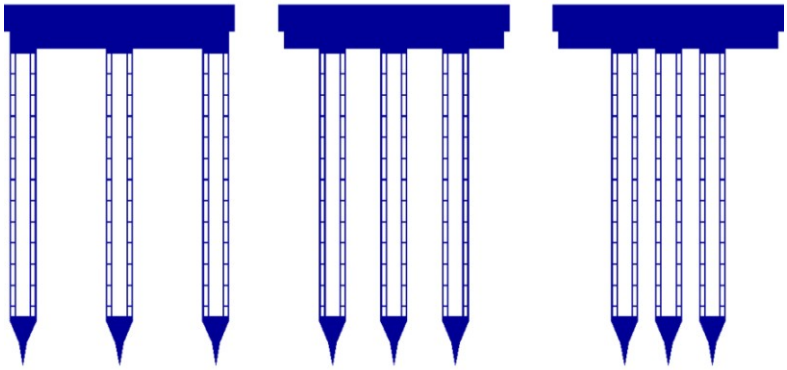


Fig. 2.25: Drawings of the multi-shank probes for the 3-D parallel probe arrays. Shank width is 300µm and spacing (gap) is 800, 400, and 200µm (left to right). Solid shank versions were also made.

The narrow-shank probes have sixteen shanks per probe. All the shanks on each probe have the same width, either 10, 5, or 3µm. However, the shank pitch varies within a probe. The center shanks have a pitch of 50µm; this is expanded as one moves laterally, first to 100µm, and then to 200µm for the outermost shanks. The variation in shank pitch was included so that the effect of this parameter on the *in vivo* response could be more systematically observed. The shank length also varies on each probe with the

center shanks the longest; this is to increase ease of insertion. The tip angle is 10°. There are two styles based on the way the shank length tapers towards the edge of the probe: staggered stair-step and curve-point; both are illustrated in Fig. 2.26.

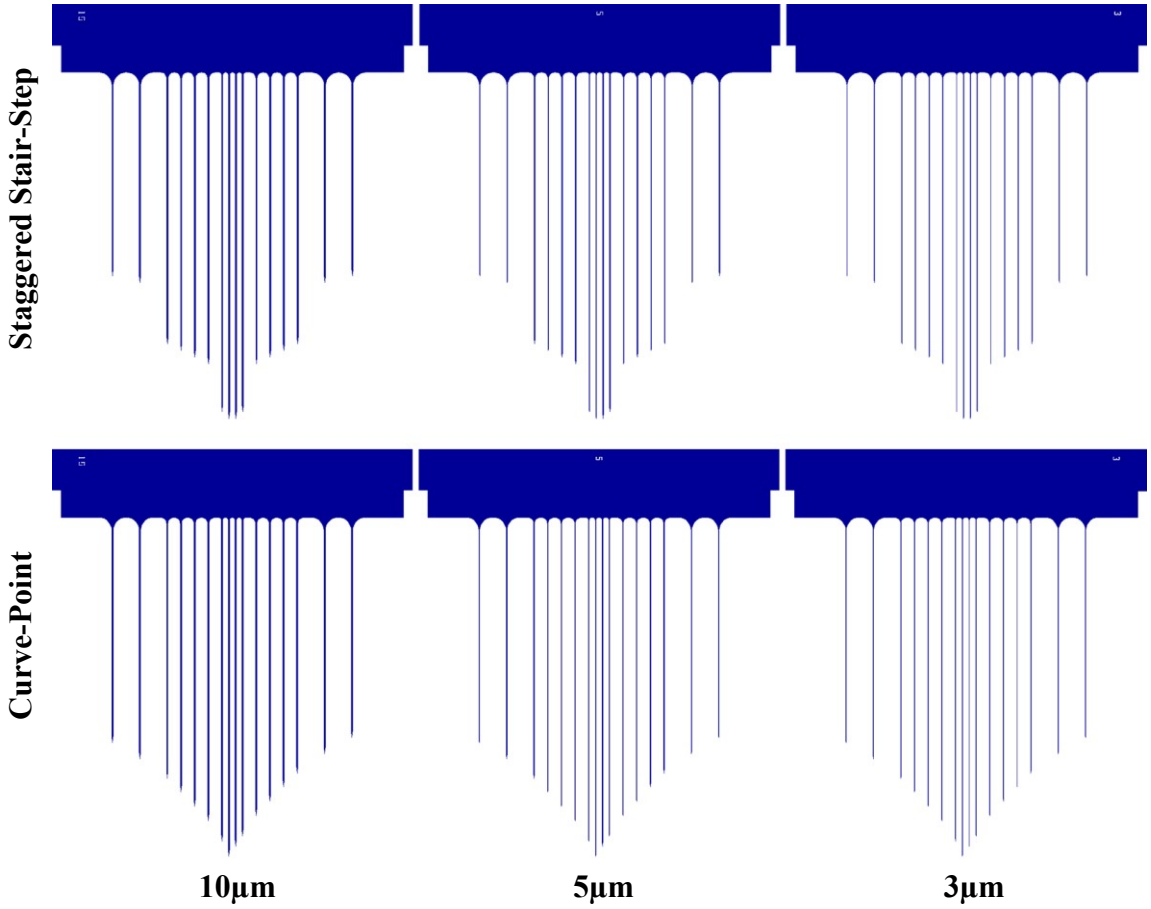



Fig. 2.26: 2-D narrow-shank probes with sixteen shanks per probe.

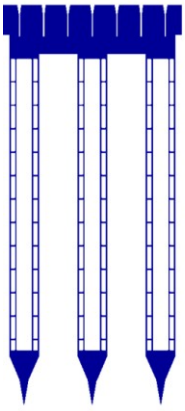
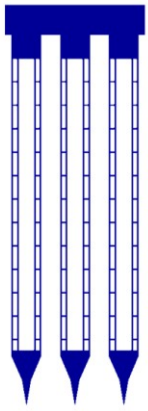
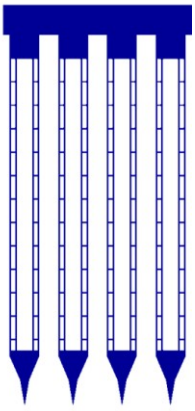
### 2.6.3 Parallel & Perpendicular Probe Arrays

Planar silicon probes have a characteristic profile of layout-controlled width and thin boron doping-controlled thickness. With the parallel probe arrays the role of in-plane shank to shank spacing and the parallel-out-of-plane probe to probe spacing may be investigated. However, another possible configuration arises when planar probes are rotated in relation to each other. Such a setup requires specifically-designed probe back-ends and platforms. In order to further consider such options, the parallel and perpendicular arrays were developed.

Three probe structures were developed for use in conjunction with the parallel and perpendicular platform: three-shank "horizontal" slot probes, three-shank "vertical" slot

probes, and four-shank "vertical" slot probes. Drawings and design details of these probes are presented in Table 2.3. The designations of "horizontal" and "vertical" were specified by convention based on the orientation of the top view of the platform during layout. The back-end designs of these probes are modified from the standard structure. The probe back-ends intended for horizontal placement have slits which allow for countersinking the vertically aligned probes. These back-end slits are 325µm deep with a 47µm wide top opening that tapers to 17µm. The back-end of the probes intended for vertical placement are only 300µm tall which enables full countersinking into the platform and horizontally placed probes; the shanks are extended by 200µm so they have the same full length as the horizontally placed devices. The array is designed so that the back-ends of all probes reach the top of the platform. Thus, with functional devices, interconnect lines could be transferred orthogonally from the probe to the platform with beam-leads.

**Table 2.3: Probe Structures for Parallel & Perpendicular Arrays**

| **Structure** | A | B | C |
|---|---|---|---|
| **Layout**<br><br>Solid shank versions were also made. |  |  |  |
| **Platform Alignment** | Horizontal | Vertical | Vertical |
| **Back-End Design** | Slits for Countersinking | Extra Low Profile | Extra Low Profile |
| **Shank Number** | 3 | 3 | 4 |
| **Shank Width** | 300µm | 300µm | 300µm |
| **Shank Spacing** | 400µm | 200µm | 200µm |
| **Shank Design** | Solid or Picket | Solid or Picket | Solid or Picket |

These devices make use of a 2200µm by 2200µm platform footprint illustrated in Fig. 2.27. The platform retains the top and bottom slot structure; however, the slots are arranged both horizontally and vertically, when viewing the platform from the top.

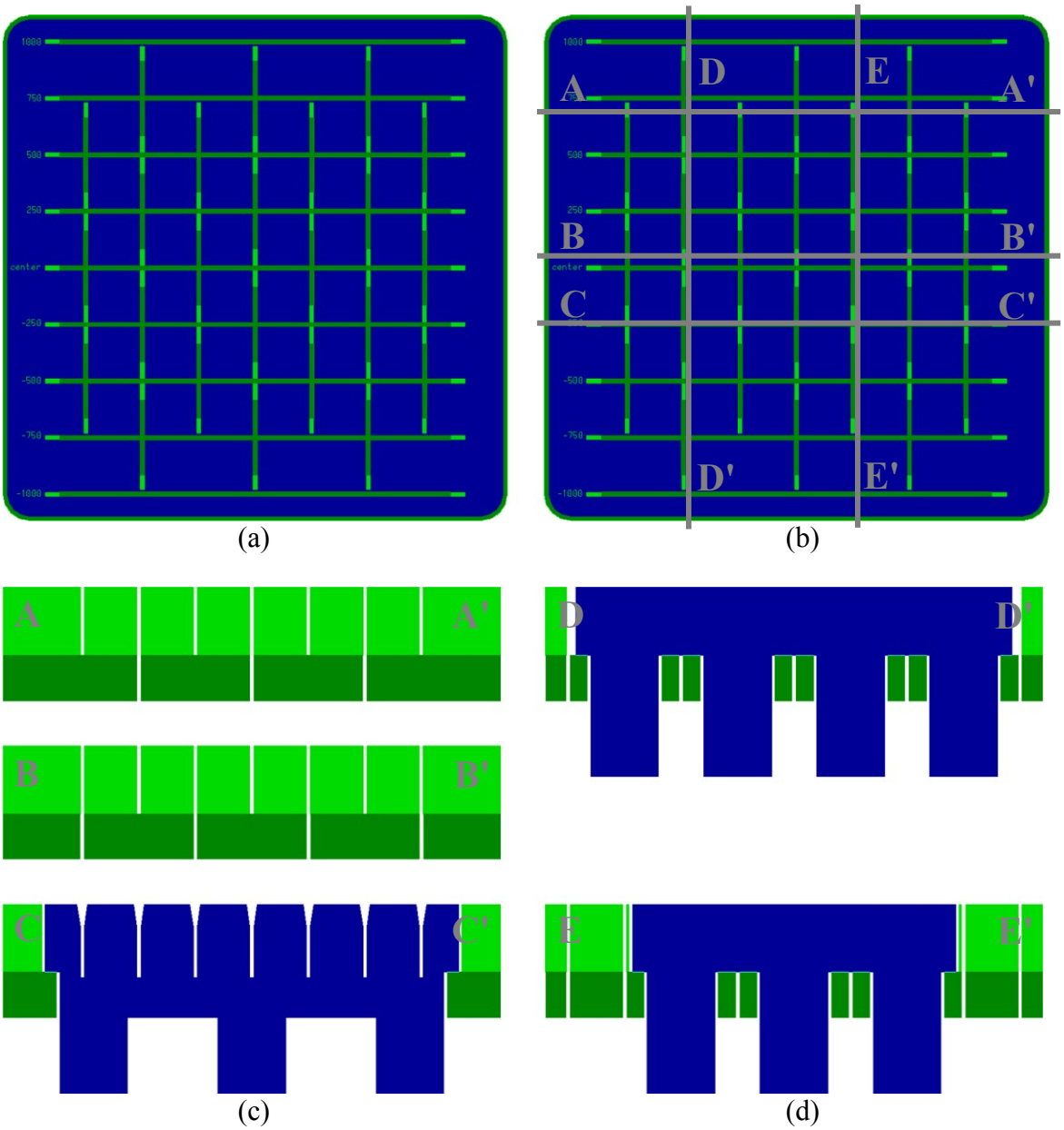


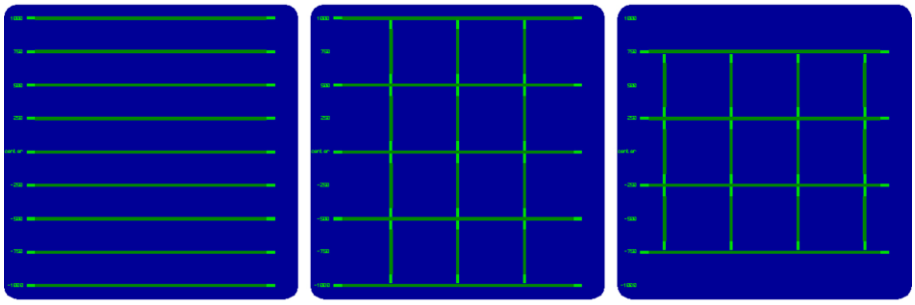

Fig. 2.27: Probe platform for simultaneous parallel and perpendicular probe arrangement. Platform (a) layout (b) marked to illustrate the (c) horizontal and (d) vertical cross-sections.

In order to maintain the platform integrity after slot formation, the slot design ensures all platform pieces are contiguous. The top and bottom slot etches for the

horizontal slots follow the typical design as described above; both span the width of the probe back-end so true slots are formed which go completely through the platform. However, for the vertical slots, only the top etch spans the entire width of the probe back-end; the bottom etch is defined solely around the potential shank regions.

The multi-purpose platform gives versatile options for platform population under three broad categories. The first general option is to populate only with parallel probes, either just the horizontal or just the vertical ones. This option is similar in effect to the platform designed only for parallel probe alignment. The second alternative utilizes the horizontal slot probes and the four-shank vertical slot probes. The third option is to use the horizontal slot probes and the three-shank vertical slot probes. Further details for these categories are given in Table 2.4.

**Table 2.4: Platform Population Options for Parallel & Perpendicular Arrays**

| **Structure** | **Option I: Parallel Probes Only** | | **Option II: Perpendicular A** | | **Option III: Perpendicular B** | |
|---|---|---|---|---|---|---|
| **Slots Potentially Used** |  | | | | | |
| **Probes** | **Pitch** | **Max #** | **Pitch** | **Max #** | **Pitch** | **Max #** |
| **"Horizontal" Slot Probes** | 250µm | 9 | --- | --- | --- | --- |
| | 500µm | 5 | 500µm | 5 | 500µm | 4 |
| | 750µm | 3 | --- | --- | --- | --- |
| | 1000µm | 3 | 1000µm | 3 | 1000µm | 2 |
| | None, Use Vertical | | --- | | --- | |
| **"Vertical" Slot Probes** | None, Use Horizontal | | 4 Shanks | | 3 Shanks | |
| | 250µm | 7 | --- | --- | --- | --- |
| | 500µm | 4 | 500µm | 3 | 500µm | 4 |
| | 750µm | 3 | --- | --- | --- | --- |
| | 1000µm | 2 | 1000µm | 2 | 1000µm | 2 |

## 2.7 Fabricated Devices and Assembled 3-D Bio-response Arrays

The fabrication of the two-dimensional multi-shank probes follows the same process as for the single shank probes discussed above. The platform slot width is capable of handling the boron-doped silicon and dielectric stack. However, to ease fabrication of the initial devices, the dielectrics were omitted; they may be included in the future without any other changes necessary. The platforms for mechanical stabilization were fabricated with deep reactive ion etching (DRIE) [59]. Photographs of individual wide-shank probes are shown in Fig. 2.28 for both the parallel only and the parallel and perpendicular arrays.

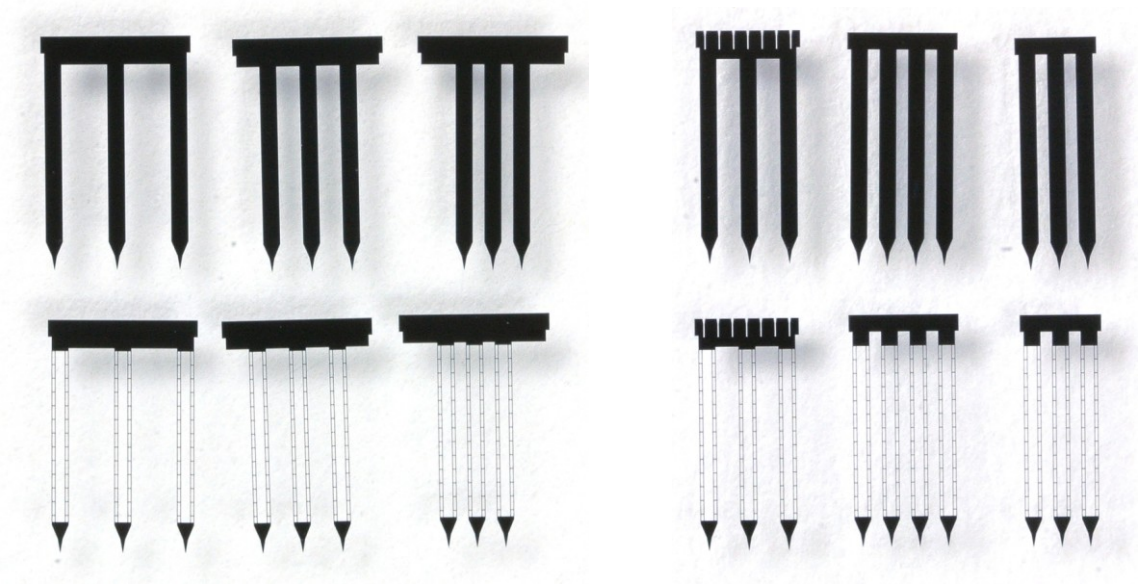


Fig. 2.28: Photographs of two-dimensional multi-shank probes for assembly in parallel arrays (left) and parallel and perpendicular arrays (right).

Fabricated narrow-shank probes are shown in Fig. 2.29. Thin boron-doped silicon probes are typically flexible out-of-plane. The narrow shanks, especially the 3μm wide shanks, are also extremely flexible in-plane. The slender shanks can spontaneously bend sideways during probe handling due to static charge as shown in Fig. 2.30. While insertion tests are necessary to validate implantability, it is possible such fine, flexible structures will be more readily accepted by the tissue. Insertion might also be assisted by strengthening the shanks with prior coating of medications that will alleviate immune response and dissolve in the tissue over time. For bio-response related studies, 200 platforms and over 650 wide and narrow multi-shank probes were sent to collaborators.

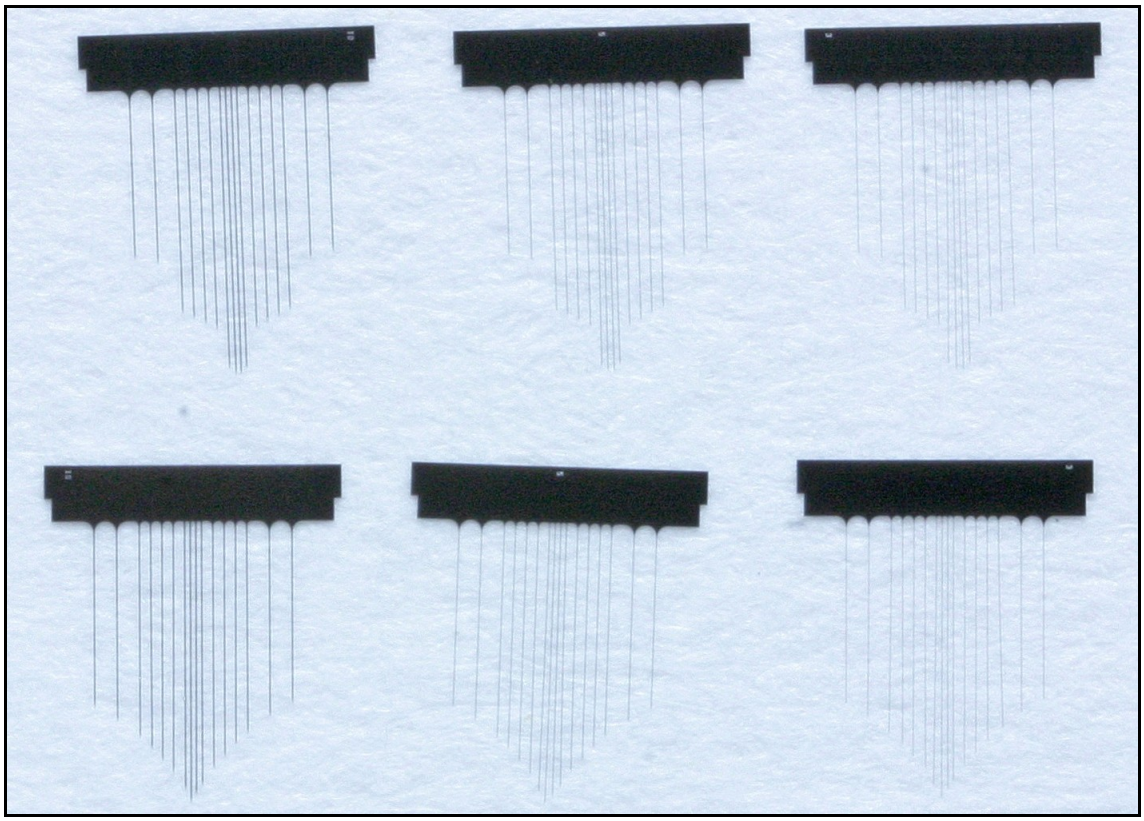


Fig. 2.29: Photo of 2-D narrow-shank (10µm, 5µm, and 3µm) probes (left to right).

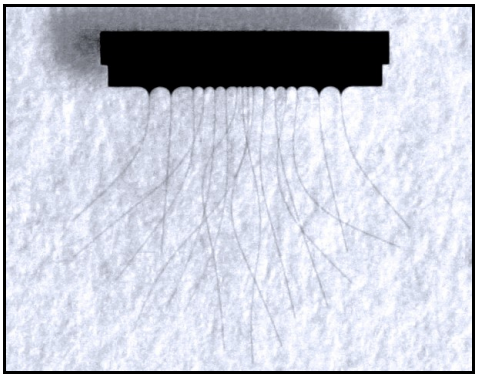


Fig. 2.30: Photograph of a 16-shank probe with 3µm wide shanks after exposing to charge to illustrate the extreme in-plane flexibility of the shanks.

Assembly of the three-dimensional arrays is straightforward. The platforms are suspended in a holder and the individual probes are aligned and inserted through the slots with the aid of a vacuum wand, micromanipulator, and microscope. For more details on three-dimensional assembly see Chapter VII. Photos of assembled wide-shank parallel-aligned probes are presented in Fig. 2.31 through Fig. 2.33. Arrays with probes arranged in both parallel and perpendicular orientation are shown in Fig. 2.34 through Fig. 2.36.

Fig. 2.31: Photo of arrays with 800µm, 400µm, and 200µm spacings (left to right).

Fig. 2.32: Photograph of 300µm-wide picket-shank 3-probe arrays with shanks and probes both spaced at 800µm, 400µm, and 200µm (left to right).

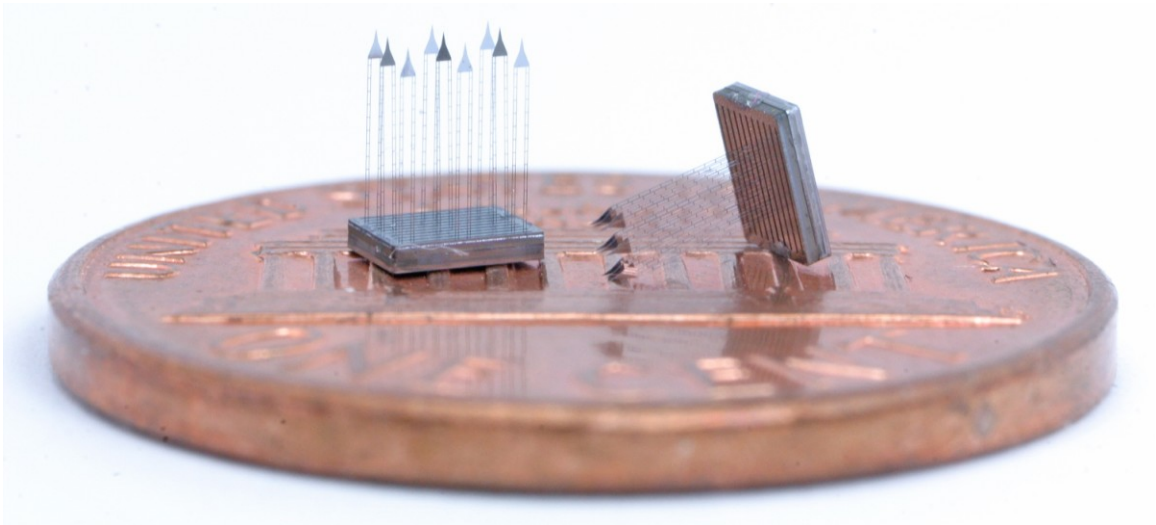
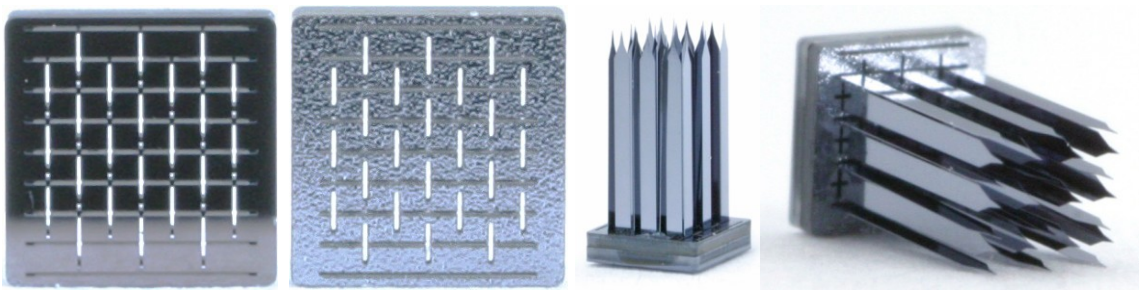
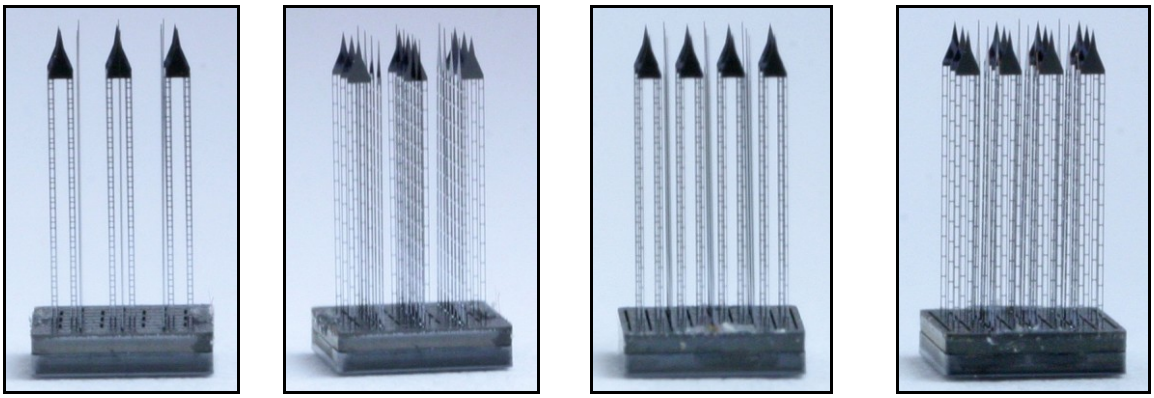


Fig. 2.33: Photograph of picket-shank 3-probe arrays with 800µm (left) and 200µm (right) shank spacing in both directions on the back of a U.S. penny.



(a) (b) (c) (d)

Fig. 2.34: Photographs of the (a) front and (b) back of the platform for parallel and perpendicular arrays and (c-d) two views of a 6-probe, solid-shank array. Three of the probes are oriented orthogonal to the other three probes.



(a) (b) (c) (d)

Fig. 2.35: Photographs of a 6-probe picket-shank array from the face of the (a-b) 3-shank "horizontal" probes and (c-d) 4-shank "vertical" probes.

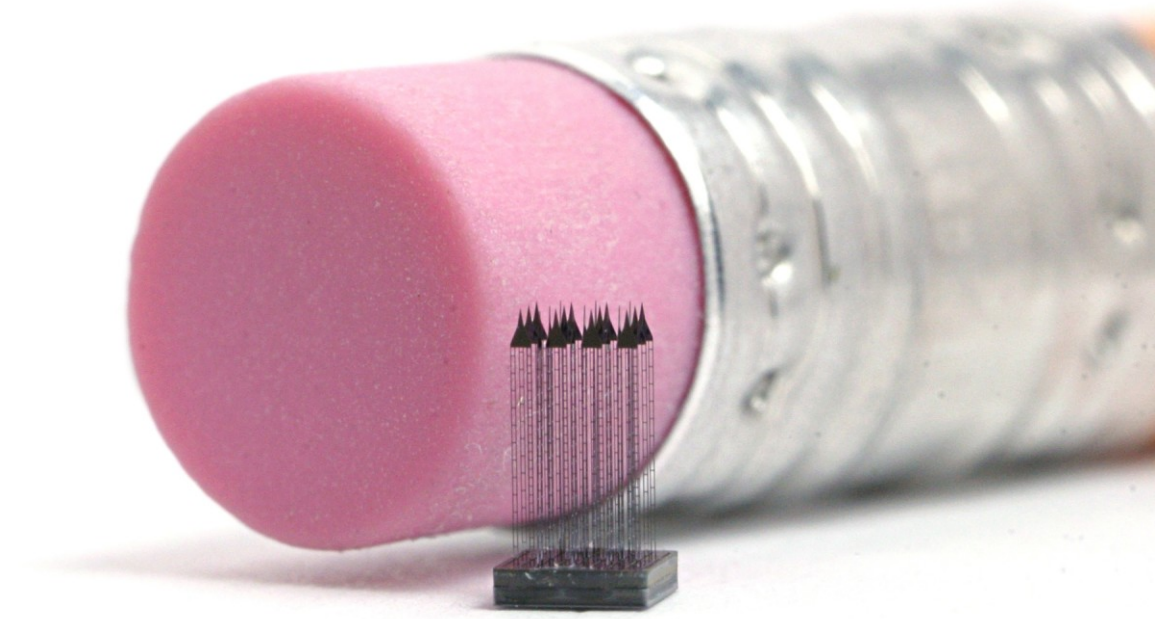


Fig. 2.36: Photograph of a 6-probe 21-shank array near the eraser of a pencil.

## 2.8 3-D Array Insertion Studies

Insertion studies were performed in order to evaluate the implantability of the 3-D wide-shank lattice arrays. This *in vivo* work in the cortex of guinea pigs was done with the assistance of Mr. James Wiler of Kresge Hearing Research Institute at the University of Michigan. Parallel arrays were tested with three to six probes, a shank spacing of 800μm, and variable probe spacings. Prior to insertion, the *dura mater* was removed. The arrays successfully penetrated the *pia mater* as shown in Fig. 2.37 and tips were fully inserted into the cortex as shown in Fig. 2.38. However, movement of the brain due to the animal's breathing caused challenges and the shanks bent under applied force, so the arrays would not readily go deeper into the cortex. Biocompatible coatings, which dissolve in the tissue after insertion, could be used to strengthen lattice architectures for implantation while maintaining the fine structure to minimize the tissue reaction.

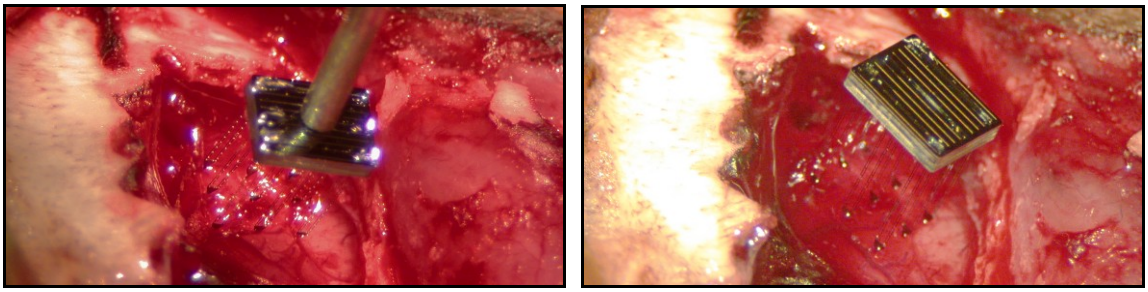


Fig. 2.37: Photographs of a 3-probe (9-shank) lattice array after penetration of the *pia*.

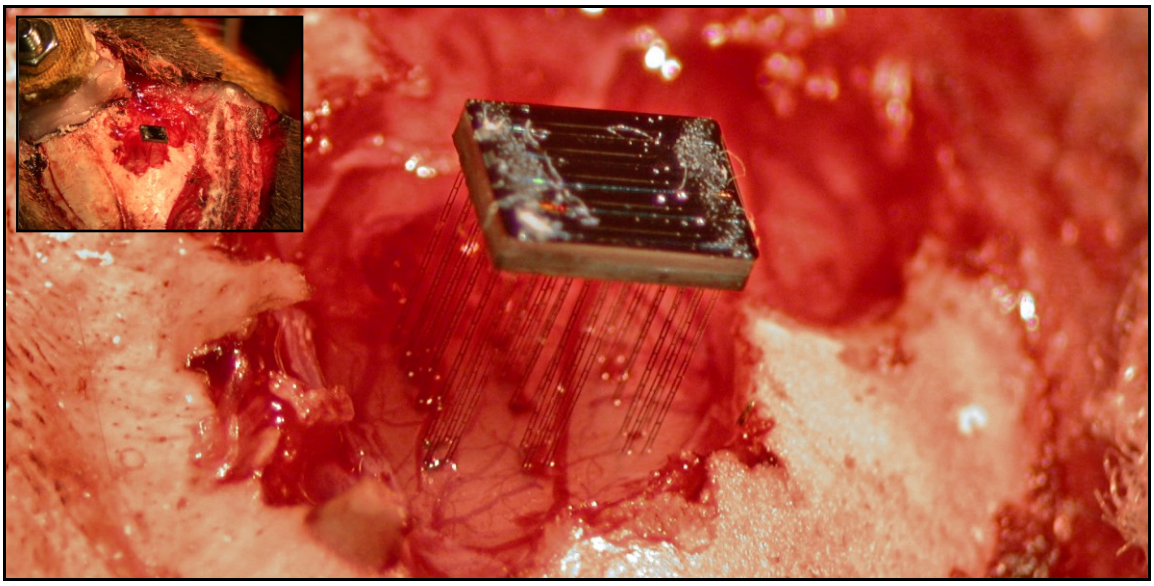


Fig. 2.38: Photographs of a 6-probe (18-shank) lattice array with the shank-tips fully inserted in guinea pig cortex.

## 2.9 Conclusions

A suite of devices has been developed in order to further immunohistological studies on chronic probe use. Both single- and multi-shank two-dimensional probes are included as well as three-dimensional arrays with parallel only and parallel and perpendicular configurations. Initial *in vivo* results show promise for the ability to modulate the tissue response through structural design. By minimizing the implanted volume of single-shank 2-D probes, while maintaining enough structural support for insertion, the chronic (8 week) immune reaction was notably mitigated in comparison to larger volume structures with identical footprints. Comparing the observed qualitative immunohistochemical results for the surrounding tissue regions and the quantitative results within the typical recording range (the first 50μm lateral to the axis of implantation) of the lattice to solid probes:

- there is less disruption in the typical density of cell nuclei (DAPI),
- the region which contains activated microglia/macrophages (ED-1) does not extend as far laterally from the device and the ED-1 density is reduce significantly (to 40.8%) in the recording range,
- the blood-brain barrier dysfunction (IgG) is dramatically lessened to 14%, and
- neuronal nuclei (NeuN) are found closer to the implanted device with chronic neuronal survival for the lattice probe (87%) substantially higher than that for the solid device (36%) as a percentage of normal NeuN density.

The technology developments of probe coatings and three-dimensional arrays have prepared the way to study the effects of implant flexibility, device permeability, surface material, and shank spacing. With multi-shank devices which have both reduced volumes and greater shank spacings, it is expected that the immune reaction will be significantly lower than that of more compact and higher-volume designs. The effect of spacing is anticipated not only to spread out the tissue response, but also to diminish it due to the increased ability of soluble factors to diffuse around the structures. The multi-shank 2-D probes and 3-D arrays developed will enable these current hypotheses involving shank spacing to be investigated.

Further studies should be pursued to make full use of the developed technology and work towards the ability to perform chronic (even lifetime) recording and stimulation.

# CHAPTER III

# CARBON NANOTUBES ON ELECTRODE SITES

Several critical issues arise out of the electrode-electrolyte interface. Recording electrodes must be capable of discriminating single unit neural activity with a high signal to noise ratio (SNR) while maintaining a stable electrode-tissue interface for chronic use [16]. Stimulation electrodes should have low impedance so that the back-voltage is manageable and the voltages on the sites remain within safe limits. These fundamentals impact the selection of geometry, material, coatings, and other aspects of the physical electrodes. In spite of progress in neural array technology, researchers are still exploring novel electrode options to reduce site impedance, counter poor SNRs, and enable dependable chronic functionality. The prospect of incorporating carbon nanotubes (CNTs) on electrodes is one possible direction for electrode innovation [91-96]. Notable CNT-related results include a decrease in site impedance and noise [91, 92], an increase in network activity [97], and the anchoring of neural cells to CNTs [95]. The means for CNT production, modification, and incorporation are diverse, which complicates study comparison and cytotoxicity designations. However, some research has shown promising initial results for CNTs as potentially biocompatible [92, 98-101].

This chapter discusses possibilities and challenges of CNT integration on electrodes with the boron-doped probe fabrication process through two distinct methods: dip-coating and *in situ* growth. This work was part of a collaborative effort with Prof. A. John Hart (Mechanosynthesis Group, Mechanical Engineering, University of Michigan) and his laboratory group, in particular Ms. Megan J. Roberts, who performed CNT growth and took the scanning electron microscope (SEM) images, and Dr. Yongyi Zhang, who prepared the dip-coating suspensions and catalyst depositions. MEMS fabrication was done by Dr. Onnop Srivannavit at the University of Michigan Lurie Nanofabrication Facility. SEM images were taken at the University of Michigan North Campus Electron Microbeam Analysis Laboratory (EMAL).

## 3.1 Electrode Site Considerations

Three important electrode parameters are the site impedance, the signal-to-noise ratio of recordings, and the chronic viability of the electrode. This section overviews aspects related to each of these parameters.

### 3.1.1 Electrode Site Impedance

Site impedance is the term typically applied to the measured impedance of the whole path including the probe packaging, electrode site, *in vitro* or *in vivo* electrolyte and (large) remote return electrode. While this impedance is frequency dependent, for neural applications the value at 1kHz is typically reported. Small, iridium electrode sites can have an impedance on the order of 0.5–5MΩ or larger. Carbon nanotube incorporation increases the effective surface area for a given geometric site area [16] and thus decreases the site-tissue impedance.

Electrode impedance is a vital factor in stimulation applications, especially those with a low-voltage supply. If the ideal back voltage (the voltage ideally generated at the output of the current source due to the selected current magnitude and load impedance) exceeds the current source voltage swing then the output current may be less than anticipated. For example, even with a low stimulation current of 1μA, if the selected electrode site has a 5MΩ impedance, then the ideal back voltage would be as high as 5V. In reality, the voltage would saturate based on the power supply and compliance voltage of the current source and less current would flow than that for which the current source was programmed.

Another factor that requires low site impedance in stimulation applications is the limit for safe stimulation. In order to ensure that charge transfer is purely capacitive or that only reversible reactions occur at the electrode-electrolyte interface, the voltage at the electrode must be kept within the water window (the potentials at which hydrogen and oxygen gases are formed). In calculating the possible range of safe current, the impedance of the interconnect lines should also be taken into account so that the actual voltage at the interface is determined rather than the voltage at the output of the current source.

### 3.1.2 Signal to Noise Ratio

Reduced impedance is expected to improve the signal to noise ratio [13, 16] and may also enable smaller site areas, leading to enhanced single unit recording and more precise unit localization. Thermal noise is a function of impedance as $V_{rms} = \sqrt{(4KTR\Delta f)}$ where k = Boltzmann's constant, T = temperature, R = impedance, and $\Delta f$ = bandwidth [13]. With a selected site material, as the site area decreases the impedance increases. This results in a trade-off between targeted single unit recording (small sites) and decreased noise (small impedance). Modifying the effective electrode area while maintaining the geometric area is a resourceful solution to this quandary.

### 3.1.3 Chronic Stability and Biocompatibility

In spite of the decades of work with micromachined electrode arrays, obtaining viable long-term recording capability is still elusive [70]. CNT surface modification, both in terms of topology and material, suggests a direction for chronic tissue acceptance of the foreign device [92, 99]. While not all bio-CNT work has found seamless integration, the number of studies incorporating CNTs in bio-applications is increasing. In a study by McKenzie, et. al., astrocytes (immune cells which encapsulate implants) were seeded on *in vitro* substrates [99]. After five days, there was statistically significant greater cell density on the glass controls than on the carbon nanofiber surfaces, indicating CNT regions may mitigate the build-up of glial scar. Single-wall carbon nanotubes (SWNTs) were formed into 50–60nm thick mats with a resistivity of 1.0–1.2Ωmm, by Mazzatenta, et. al. [102]. Hippocampal neurons were cultured on the mats and displayed typical healthy morphology. Patch clamp recording revealed that electrical stimulation of the cells via the CNT-mat was possible. *In vitro* work by Gabay, et. al., showed that neurons preferentially clustered on grown-CNT electrodes over silicon dioxide substrates [92, 103]. The growth was based on titanium nitride sites with a 7nm nickel catalyst. Extracellular waveforms of spontaneous activity were recorded. Keefer, et. al., coated wire electrodes with CNTs and recorded *in vivo* in rats and monkeys [91]; however, chronic results were not presented. Tsang, et. al., electroplated CNT-Au nanocomposite onto gold sites, implanted the devices in the abdomen of moths, and were able to elicited abdomen motions with stimulation; again, full biocompatibility was not elucidated.

## 3.2 CNT Incorporation Methods and Probe Preparation

Probe development at the University of Michigan has used boron-doped silicon to define probe thickness in a wet release and to enable the implanted substrate to withstand the *in vivo* environment. For this CNT research, it was decided to maintain the boron doping and to work towards process compatible methods for incorporating CNTs on the sites. After a CNT application viability trial, two methods of CNT incorporation were pursued: dip-coating and *in situ* growth. Certain aspects of the standard probe process flow were modified to reduce the number of processing steps and better meet the needs of the CNT research. This section overviews the general process flow and subsequent sections detail the modifications made for the dip-coating and growth methods.

### 3.2.1 Probe Fabrication Overview

A schematic of the general process flow is shown in Fig. 3.1 and details are listed in Table 3.1. Blanket boron doping eliminated one mask; future runs may use selective doping without otherwise modifying the process. The bottom dielectrics were the typically used low-pressure chemical vapor deposition (LPCVD) oxide/nitride/oxide (Ox/Ni/Ox) stack. Doped polysilicon interconnect has significant lead resistance (>10Ω/□); if the site impedance is low, the polysilicon resistance could be a significant portion of the measured impedance. In order to minimize interconnect resistance, a titanium/iridium/titanium (Ti/Ir/Ti) stack was used rather than polysilicon leads. The titanium acts as adhesion layers. This stack is capable of handling the high temperature of the CNT growth. With metal already on the device, the top insulation could not be LPCVD dielectrics due to possible contamination of the LPCVD furnace. Therefore, a thick plasma-enhanced chemical vapor deposition (PECVD) oxide was used instead. The standard titanium/iridium was used for the electrode sites; this was also used for the bond pads instead of the more commonly used chromium/gold. Using the same material for the sites and pads eliminated a mask, enabled more options for later processing steps, and also limited the number of materials exposed during CNT growth. The probe shapes were defined near the end of the process with a dielectric etch followed by a front-side deep reactive ion etch (DRIE). The back-side was also thinned by DRIE before the wet release in EDP (ethylene diamine, pyrocatechol, and water).

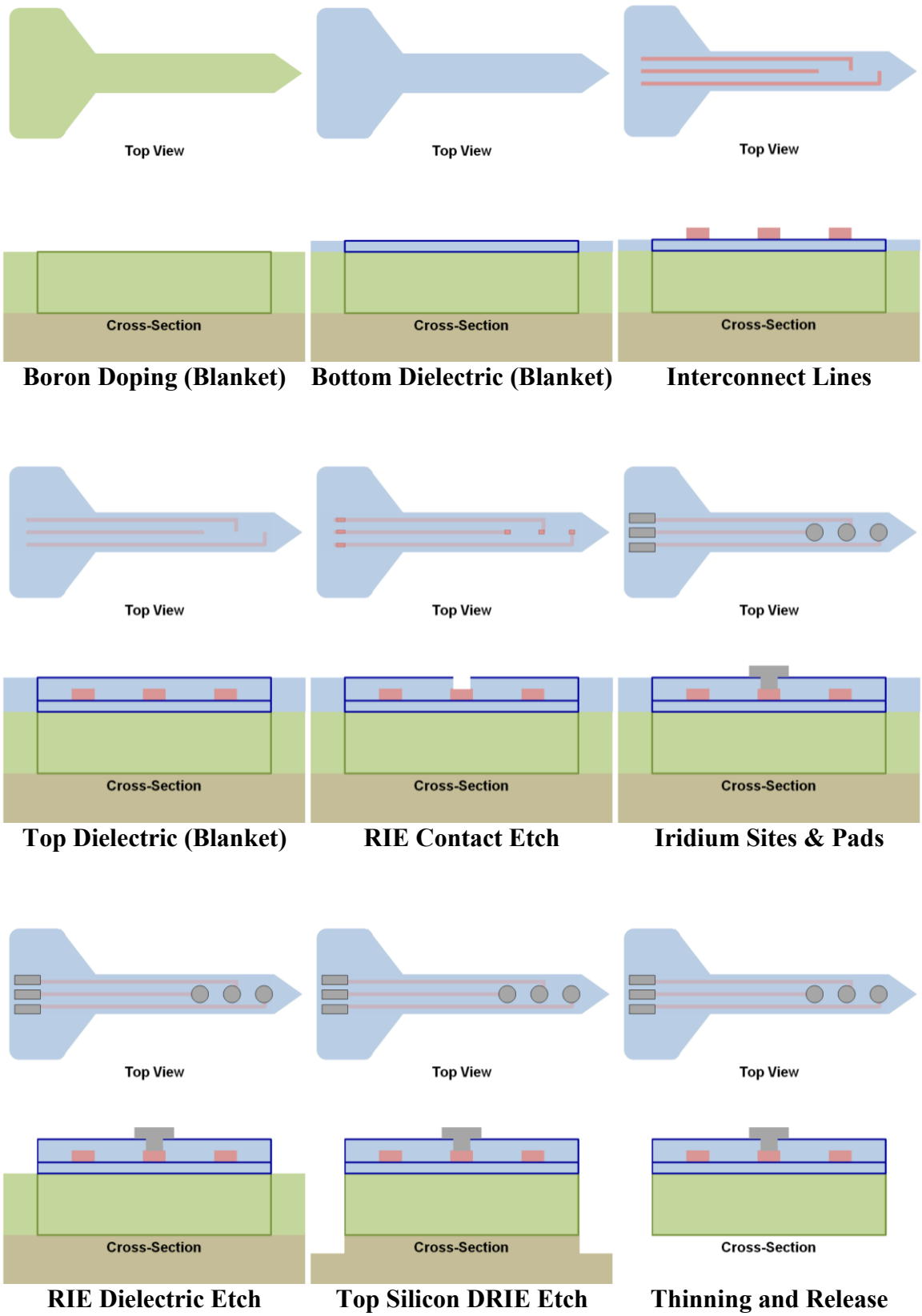



Fig. 3.1: Drawings of the general fabrication steps.

| Table 3.1: Probe Process Flow with Method Variations | | | | |
|---|---|---|---|---|
| **Purpose** | **Mask** | **Material / Comment** | **Deposit Thickness (Etch indicated by x)** | **Method** |
| Blanket Boron | | Boron | (12μm deep) | Diffusion |
| Bottom Dielectric Stack | | Pad Oxide | 1,500Å | Thermal |
| | | Oxide | 3000Å | LPCVD |
| | | Nitride | 1,500Å | LPCVD |
| | | Oxide | 3000Å | LPCVD |
| Interconnect Lines | 1. POL | Ti/Ir/Ti | 400Å/1500Å/400Å or 400Å/3000Å/400Å | Sputter / Liftoff |
| Top Dielectric | | Oxide | 1.6μm | PECVD |
| Contact Etch | 2. CON | | x | RIE |
| Sites & Bond Pads | 3. IRD | Ti/Ir | 400Å/1500Å | Sputter / Liftoff |
| Back-Side Dielectric Etch | | | x | RIE |
| CNT Catalyst✧ | 4a. CNTG | $Al_2O_3$/Fe | 100Å/35Å | Evaporation / Liftoff |
| Catalyst Protection✧❖ | 5. DEL | Cr | 1500Å | Sputter / Etch |
| Dip-Coating Mask⌖ | 4b. CNTD | Cr | 1500Å | Sputter / Etch |
| Front-Side Dielectric Etch | 5. DEL | | x | RIE |
| Front-Side Silicon Etch | | Probe Shape | x | DRIE |
| Back-Side Silicon Etch | | Wafer Thinning | x | DRIE |
| Wet Release❖ | | | x | EDP |
| Remove Catalyst Protection✧❖ | | | x | Cr Etch |
| CNT Growth✧ | | CNTs | | Growth |
| Dip-Coating⌖ | | CNTs | | Dip-Coat / Liftoff Cr Etch |

✧These steps are omitted when preparing probes for CNT incorporation by dip-coating.
⌖These steps are omitted when preparing probes for CNT incorporation by growth.
❖These steps are omitted when releasing probes by DRIE.

### 3.2.2 Overview of CNT Probe Design

For post-processing handling purposes, the probes designed for CNT incorporation were tethered to a backbone in a comb configuration, as illustrated in Fig. 3.2. Once the CNT incorporation was completed, the probes were removed from the backbone by snapping the silicon connection tabs. Fourteen designs were included with sixteen iridium-based sites per probe in five circular site sizes (7.5, 15, 30, 60, 120μm diameter). The dip-coating (CNTD) and catalyst (CNTG) masks had solid sites following the iridium site sizes as well as other geometries.

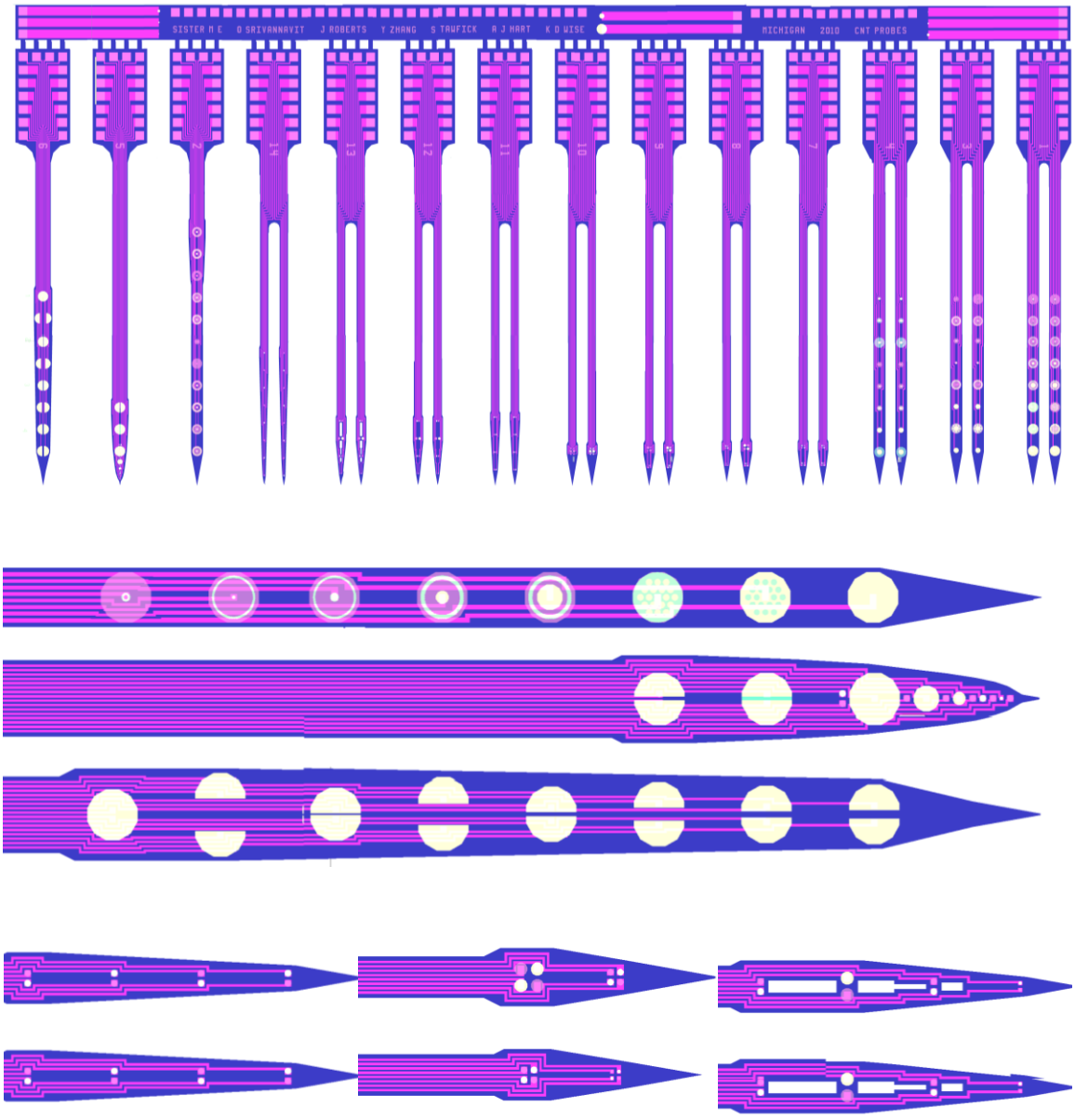



Fig. 3.2: Comb layout of CNT-probes on handling backbone and site close-ups

### 3.2.3 Process Modification for CNT Incorporation by Dip-Coating

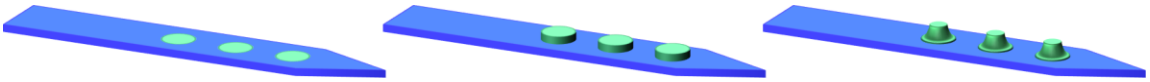
In order to deposit CNTs from a water suspension onto the probes and then pattern the layer, three methods were considered: spinning, evaporation, and dip-coating. Initial trials indicated that there were greater challenges with the first two options than with the dip-coating. When spinning the suspension, very little adhered to the sample and most was lost. In evaporation trials, either liftoff of the deposited CNTs was not achieved or whole regions lifted off including those which were not intended to liftoff. It was presumed that this was due to the fact that the deposited CNTs formed an entwined mesh, and the regions over the sites and over the mask were not sufficiently separated; the length of the CNTs may have also played a role in the liftoff issues. With dip-coating, multiple layers built up over the course of many dips. Therefore, the network of dispersed CNTs was not (presumably) as intertwined as in the evaporation method.

The dip-coating procedure required a mask to be patterned before the probes were released from the wafer, so the mask must survive in EDP. Initial tests were done on non-released probes with a photoresist (PR) mask as further described in Section 3.3.2. However, since photoresist can not withstand the wet release it was excluded as a final option. Chromium (Cr) was selected since it had previously been proven that it endures in EDP when used as an adhesion layer under gold bond pads. When incorporating this mask into the process flow it was sputtered and patterned before the front-side dielectric etch. The dip-coating mask (CNTD) was used to pattern the chromium layer to open the sites on to which CNTs were to be deposited. The dielectric mask (DEL) was subsequently used to remove the chromium layer in-between devices and then to also remove the dielectrics in the field regions.

After probe release, the devices were dip-coated. Initial work used a syringe pump to pull the sample out of the CNT suspension but required manual lowering for each dip. In subsequent development of the setup, A LabVIEW program, written by Mr. Neil K. Dhingra, automated the dip-coating by controlling a syringe pump (WPI Micro4). The number of dips, dip distance, and speed were selectable. After dipping, a chromium etch was performed in order to liftoff the CNTs in the regions other than the selected sites. After rinsing the device it was ready for impedance measurements.

### 3.2.4 Process Modification for CNT Incorporation by *In Situ* Growth

The CNT grow steps are shown conceptually in Fig. 3.3 [104]. The alumina and iron ($Al_2O_3$/Fe) catalyst layers were deposited by evaporation and patterned by liftoff. The catalyst was annealed in the CNT furnace and growth was performed around 700°C in a hydrocarbon atmosphere. Five growth times were used in this work to date: 10min, 2min, 1min, 45s, and 30s. On-going development is working to achieve shorter CNT forests, more suitable for *in vivo* implantation. On selected devices, the nanotubes were also densified by Mr. Sei Jin before impedance measuring.



(a) (b) (c)

Fig. 3.3: Conceptual drawings of the CNT growth stages: (a) the catalyst ($Al_2O_3$/Fe) deposition and patterning, (b) annealing and growth, (c) and densification.

Process flow development for the *in situ* growth presented several significant challenges, specifically regarding the acceptable base layers, catalyst adhesion, and EDP survival. The materials under the catalyst can effect growth. Substrate trials verified that Ti/Ir/$Al_2O_3$/Fe stacks would grow CNTs. However, Ti/Fe and Ti/Ir/Fe stacks did not exhibit growth and Ti/$Al_2O_3$/Fe only grew on some samples. Stacks of Ti/Ir/Ti/$Al_2O_3$/Fe in which the center titanium layer was thin (~300Å) also had growth.

Initially the catalyst was patterned with a separate mask after the sites were defined. Although some catalyst was missing after the patterning step due to poor adhesion, the remaining catalyst grew CNTs on non-released probes. Due to the adhesion issue or pinhole exposure to EDP, effectively none of the catalyst survived the release even with a protective mask. To reduce the adhesion problems, the second trial used recessed sites (~5000Å deep) and patterned the iridium and catalyst with a single liftoff. Catalyst adhesion on non-released probes was significantly higher in this version.

Initial studies found that the catalyst will not survive the EDP etch, but will remain and grow CNTs after a chromium etch. Therefore, a sputtered chromium layer was used to mask the alumina/iron. The chromium was patterned with the dielectric mask to remove it from the field regions before the front-side dielectric etch. After the wet release, the chromium mask was removed.

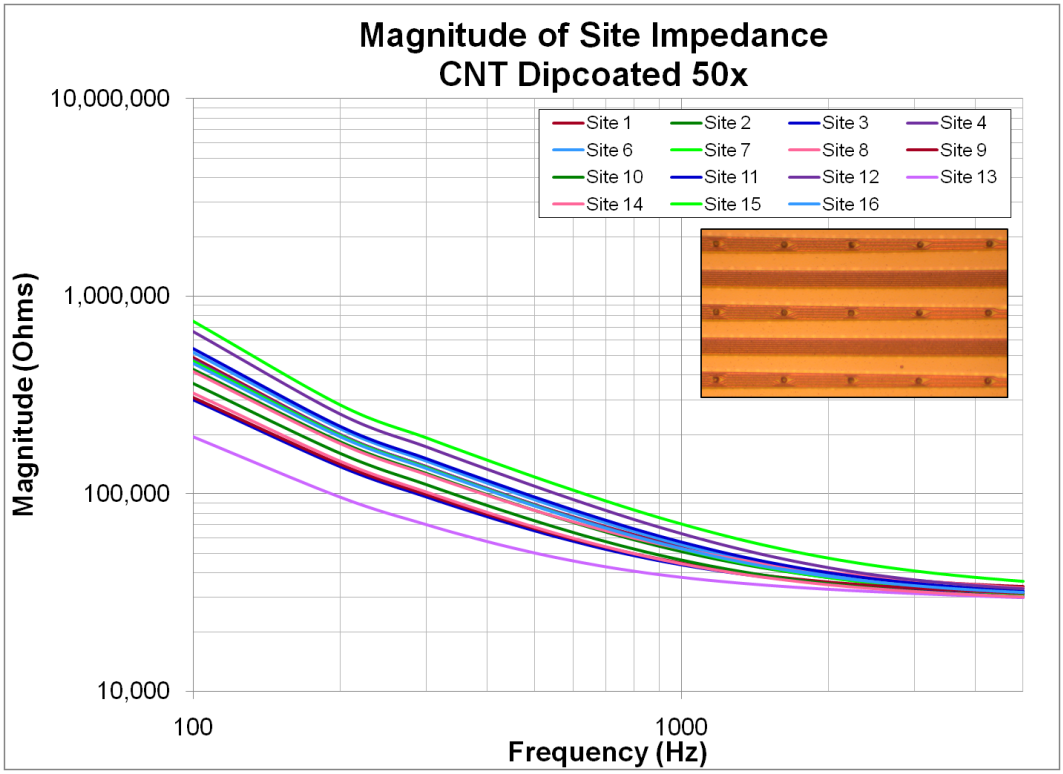
## 3.3 Results

### 3.3.1 CNT Application Viability Trial

As a first test, probe shanks were dipped into a suspension of CNTs in water in order to obtain a partial coating; the probes were heated and then air dried overnight before post-impedance measurements were taken. The electrode impedance of ten sites (selected after CNT deposition) dropped from an average of 1.63MΩ to 0.11MΩ at 1kHz. Additionally, no visual change was observable in the CNT coated sites after soaking in room temperature saline for almost a week. While no attempt was made during this trial to pattern the CNT film, the decrease in impedance by a factor of fourteen encouraged efforts to pursue process integration.

### 3.3.2 CNT Dip-Coating on Non-Released Probes

Some experiments focused on impedance measuring of coated sites without first bringing the structures through the release process. Some of these used polysilicon interconnect and a thick (3μm) photoresist mask, which had several advantages. Photoresist is relatively hydrophobic so CNTs did not tend to deposit on the photoresist. The thick mask formed wells around the sites which may have enabled a larger droplet of the suspension to form per dip. These two factors contributed to faster and more selective site coating with the photoresist mask than chromium. Additionally, a short (<1min) low-power ultrasonication in acetone was sufficient to liftoff the photoresist and the site edges looked smooth (as patterned). Fig. 3.4 and Fig. 3.5 show the measured impedance and insets of the CNT patterned sites on two structures which used a photoresist mask. For comparison, Fig. 3.6 presents measured impedance values of iridium sites with areas of 177$\mu m^2$ and of 1000$\mu m^2$. The 1kHz impedance value of these CNT sites is about one order of magnitude lower than the impedance of iridium sites with the same geometric area as shown in Fig. 3.7. With a chromium mask (1500Å) on non-released probes, the chromium coated more readily with CNTs than the exposed sites. The site edges were jagged, perhaps indicating an intertwining of the CNTs on and off the site edge since the step height was significantly smaller than on the photoresist mask version.



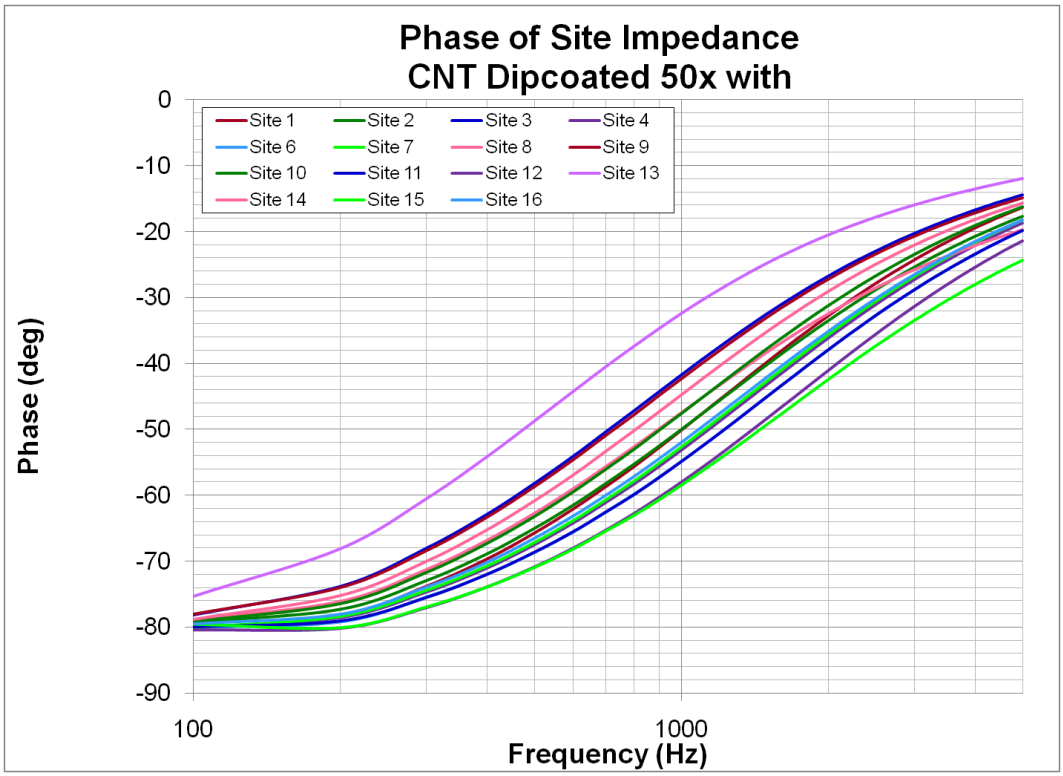




Fig. 3.4: Measured impedance of CNT dip-coated sites on a non-released structure with an electrode geometric area of 177μm$^2$ and a photoresist liftoff mask.

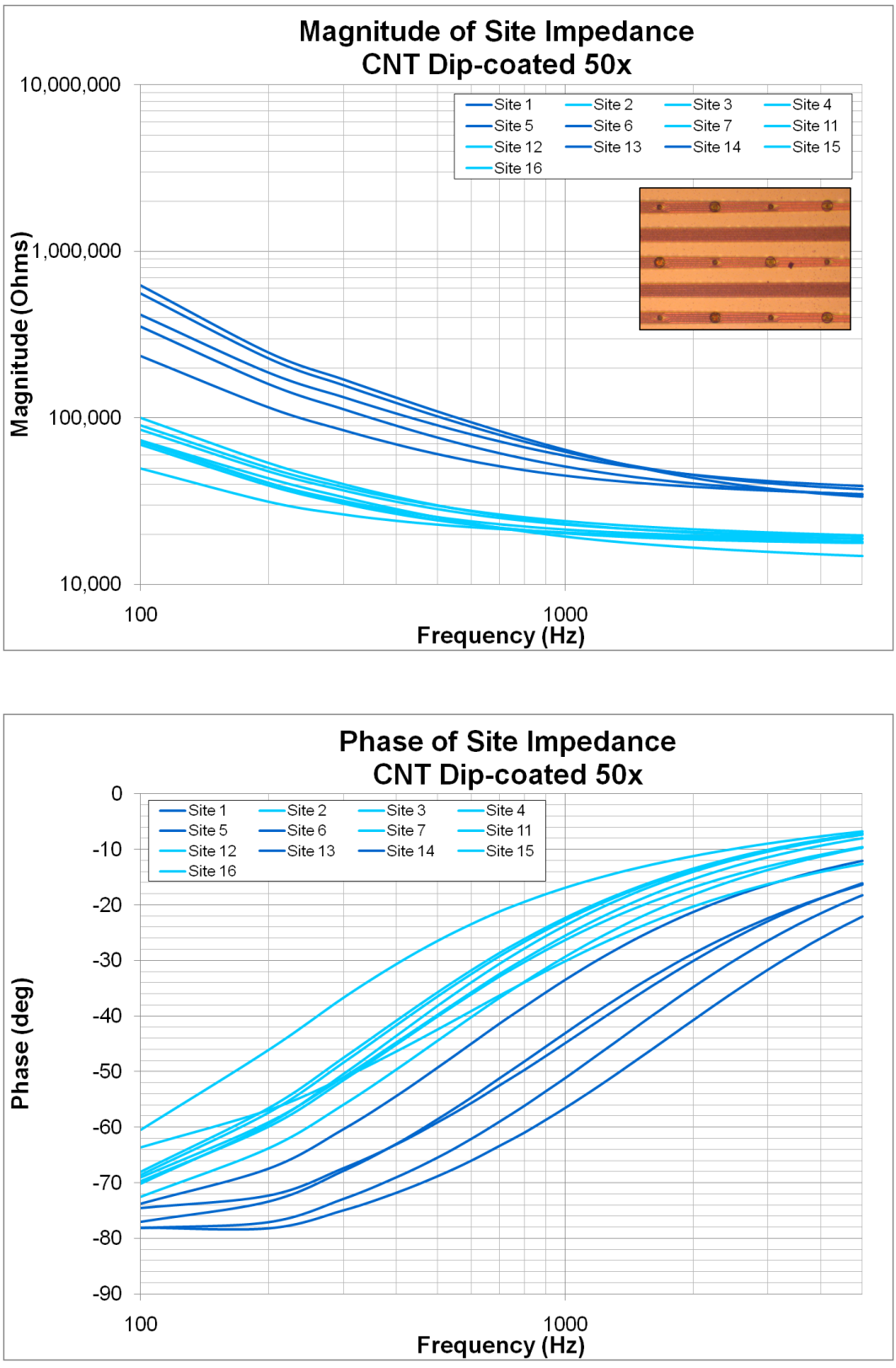



Fig. 3.5: Measured impedance of CNT dip-coated sites on a non-released structure with two electrode sizes, 177µm$^2$ (dark blue) and of 1000µm$^2$ (light blue).

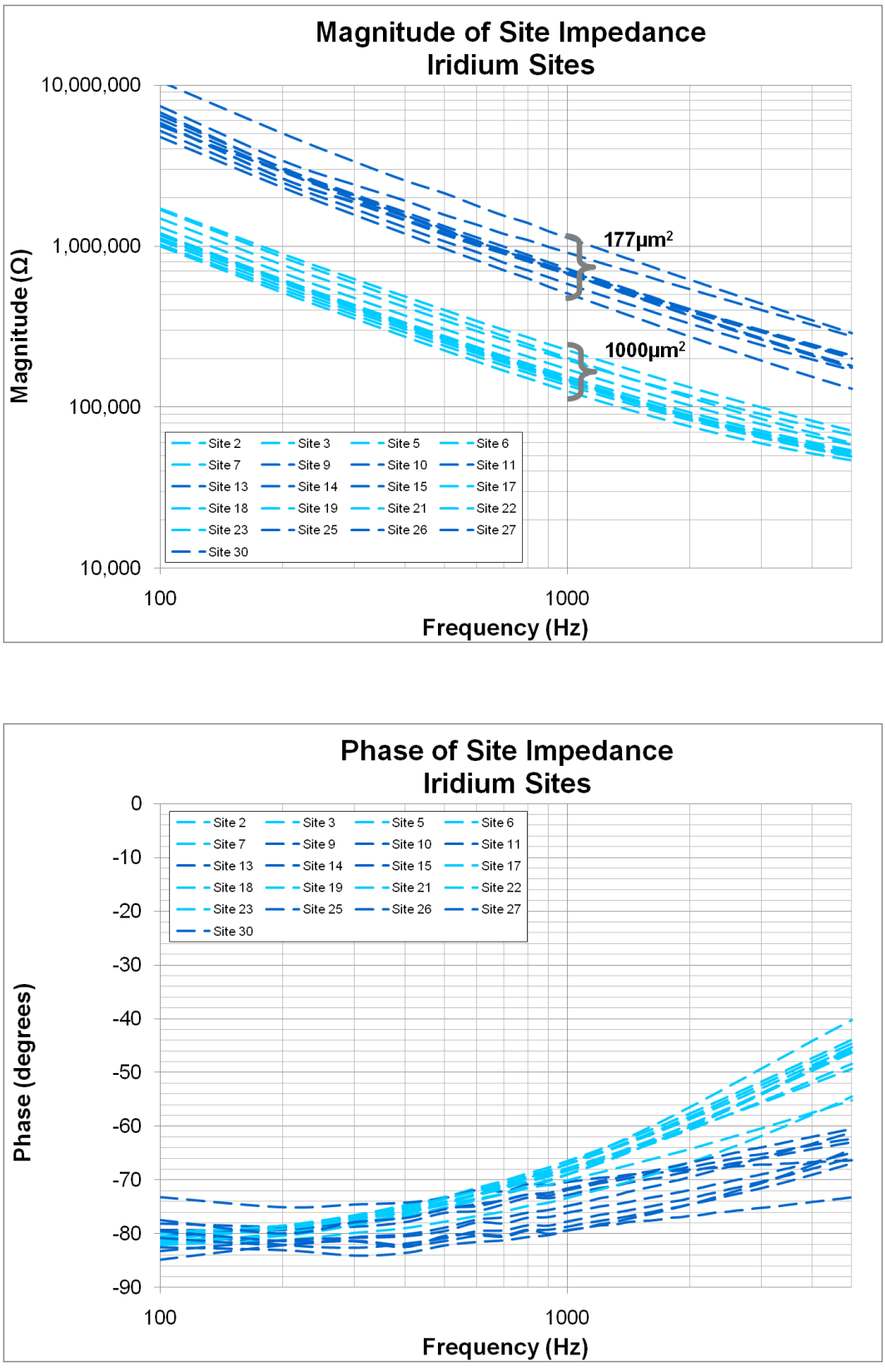



Fig. 3.6: Measured impedance of iridium control sites on a probe with two site sizes, 177µm$^2$ (dark blue) and of 1000µm$^2$ (light blue).

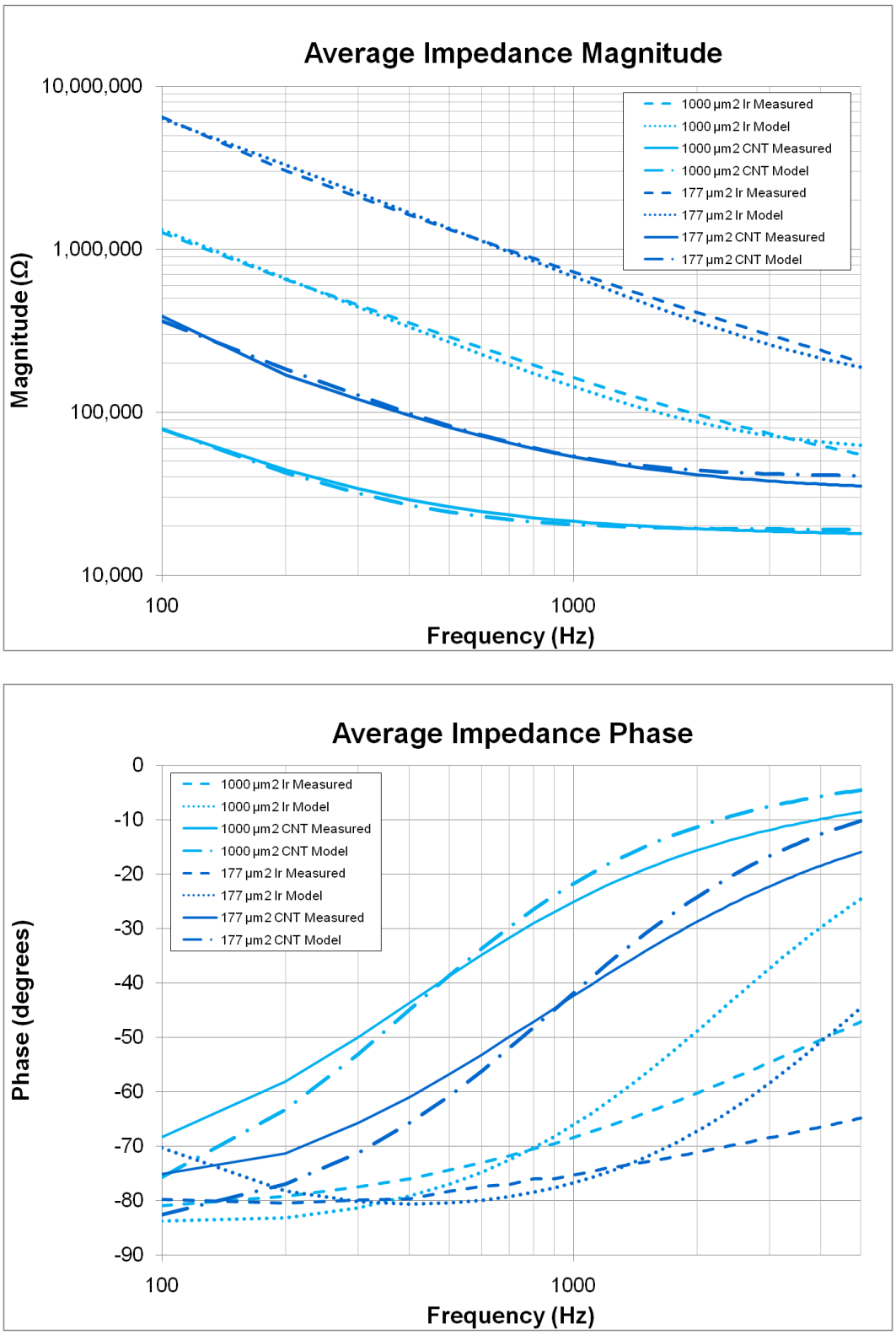
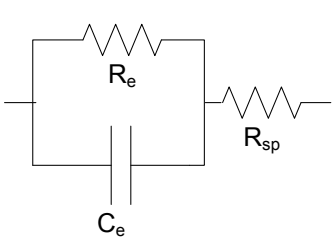



Fig. 3.7: Average of measured impedances of good iridium sites (dashed) and CNT dip-coated sites (solid), with areas of 177µm$^2$ (dark blue) and 1000µm$^2$ (light blue). Parameter-fit with Randles model is also shown, see Section 3.3.3.

### 3.3.3 Equivalent Circuit Modeling for Non-Released Dip-Coated Sites

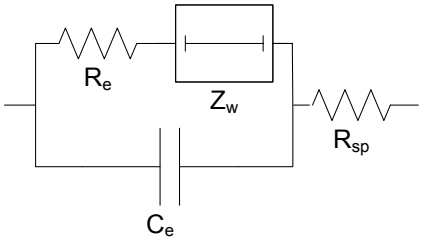
Randles model, shown in Fig. 3.8a, is one of the basic models for electrode-electrolyte interfaces [105, 106]. The associated transfer function is derived in Fig. 3.9. This model was applied to the photoresist-masked non-released CNT dip-coated sites through a Matlab program by Mr. Neil K Dhingra. The zero was estimated from the forty-five degree point of the phase graph. In order to accurately determine the pole location (and hence Re), lower frequency *in vitro* measurements are needed. From the value the magnitude plot asymptotically approaches at high frequencies, the value of Rsp, the series resistance of the interconnect and spreading resistance of the electrolyte, can be estimated. Fig. 3.7 includes the model graphs; the impedance is well matched, but the phase is not. By adding additional components, such as the Warburg constant phase element and an inductance, the modeling can be improved [105, 106].




(a)

| Extracted Parameter Values | | | | |
|---|---|---|---|---|
| | 1000µm² | | 177µm² | |
| | Ir | CNT | Ir | CNT |
| Rsp | 57kΩ | 19kΩ | 134kΩ | 40kΩ |
| Ce | 0.4µF | 7.5µF | 0.9µF | 1.6µF |

(b)




(c)

Fig. 3.8: Diagrams for modeling electrode-electrolyte interface: (a) Randles model with (b) parameter values and (c) with the Warburg constant phase element.

$$R_{sp}+\frac{\frac{R_e}{sC_e}}{R_e+\frac{1}{sC_e}}=R_{sp}+\frac{R_e}{sC_eR_e+1}=\frac{R_{sp}C_eR_es+R_{sp}}{sC_eR_e+1}+\frac{R_e}{sC_eR_e+1}=\frac{sC_eR_eR_{sp}+R_e+R_{sp}}{sC_eR_e+1}$$

$$=\frac{sR_{sp}+\frac{1}{C_e}+\frac{R_{sp}}{C_eR_e}}{s+\frac{1}{C_eR_e}}=\frac{s+\frac{1}{C_eR_{sp}}+\frac{1}{C_eR_e}}{\frac{1}{R_{sp}}(s+\frac{1}{C_eR_e})}=R_s\frac{s+\frac{1}{C_eR_{sp}}+\frac{1}{C_eR_e}}{s+\frac{1}{C_eR_e}}$$

Fig. 3.9: Derivation of the transfer function of Randles model (by N. Dhingra).

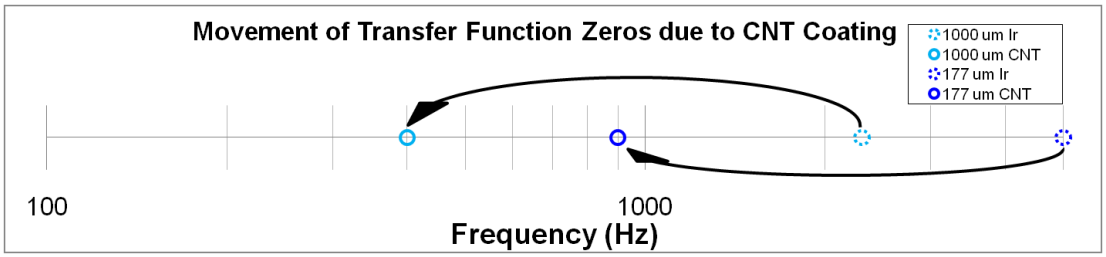



Fig. 3.10: Graph showing movement of the zeros in the modeled transfer function.

### 3.3.4 CNT Dip-Coating on EDP Released Probes

The dip-coating process with a chromium mask was performed on released probes. Raman spectroscopy confirmed that sites contained CNTs; one Raman spectrum is shown in Fig. 3.11. Impedance graphs are presented in Fig. 3.13 and Fig. 3.14 for five sites areas; the reduction was not as significant as that for the non-released probes with photoresist mask. This may be due in part to a processing issue which caused baked photoresist to remain on some of the probe surface after release. Probes were implanted in guinea pig auditory cortex and recorded multi-unit activity elicited using white noise bursts as acoustic stimulus; neural waveforms are presented in Fig. 3.12. Visual inspection verified that CNTs were still on the electrode sites after explantation.

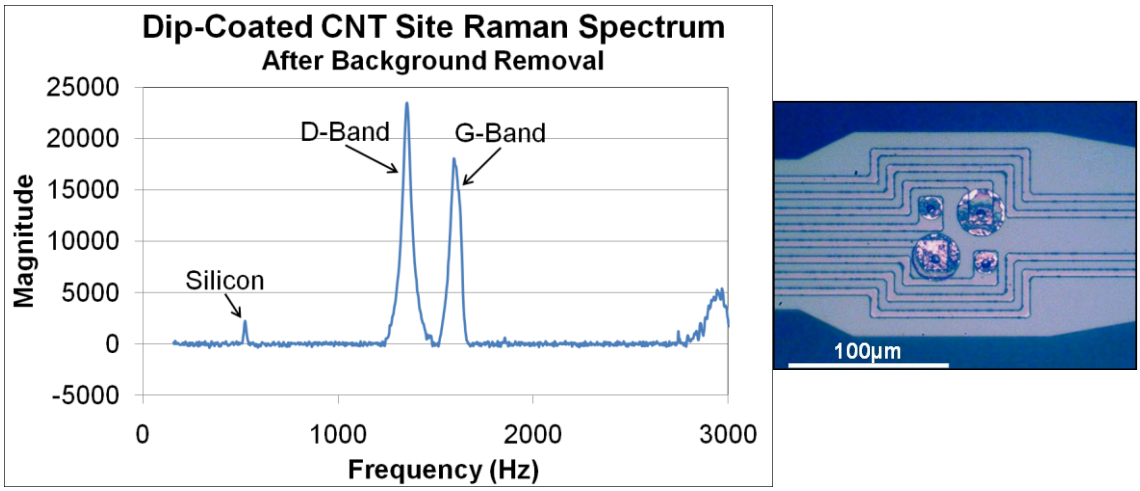



Fig. 3.11: Raman spectrum and photograph of released-probe CNT dip-coated sites.

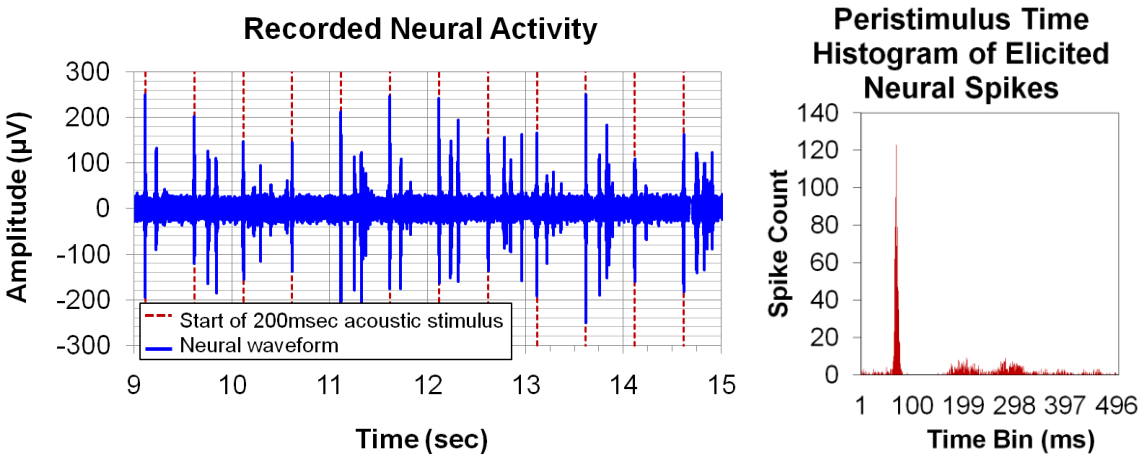
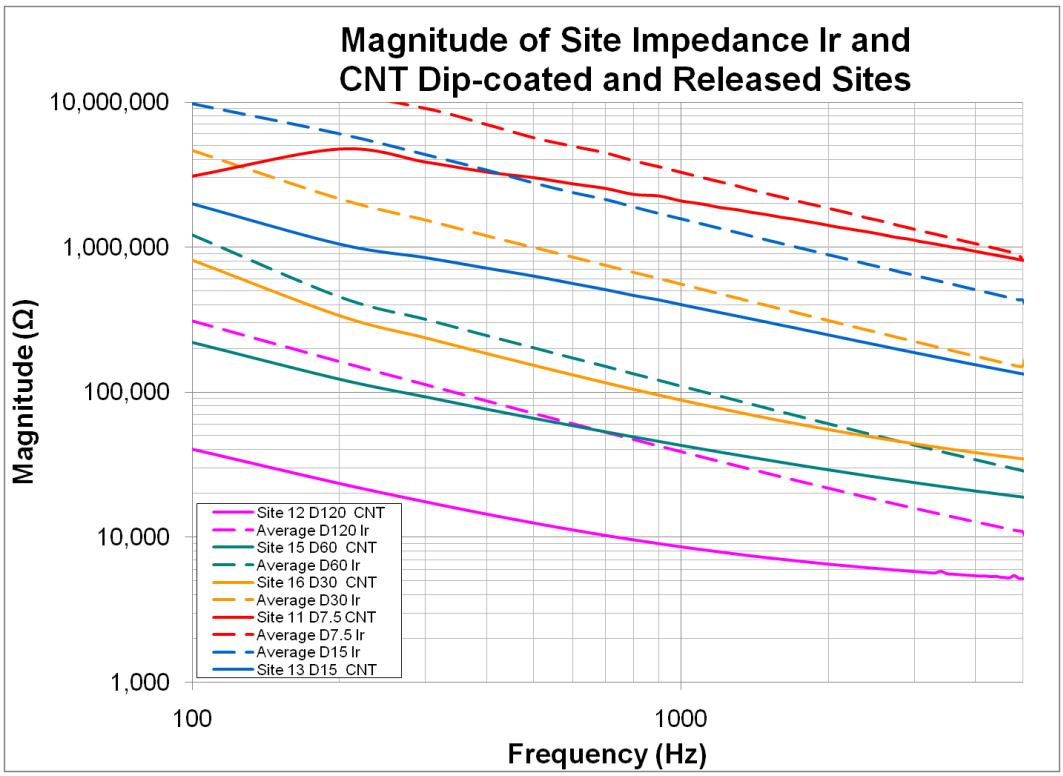



Fig. 3.12: *In vivo* neural recordings with CNT dip-coated probe.



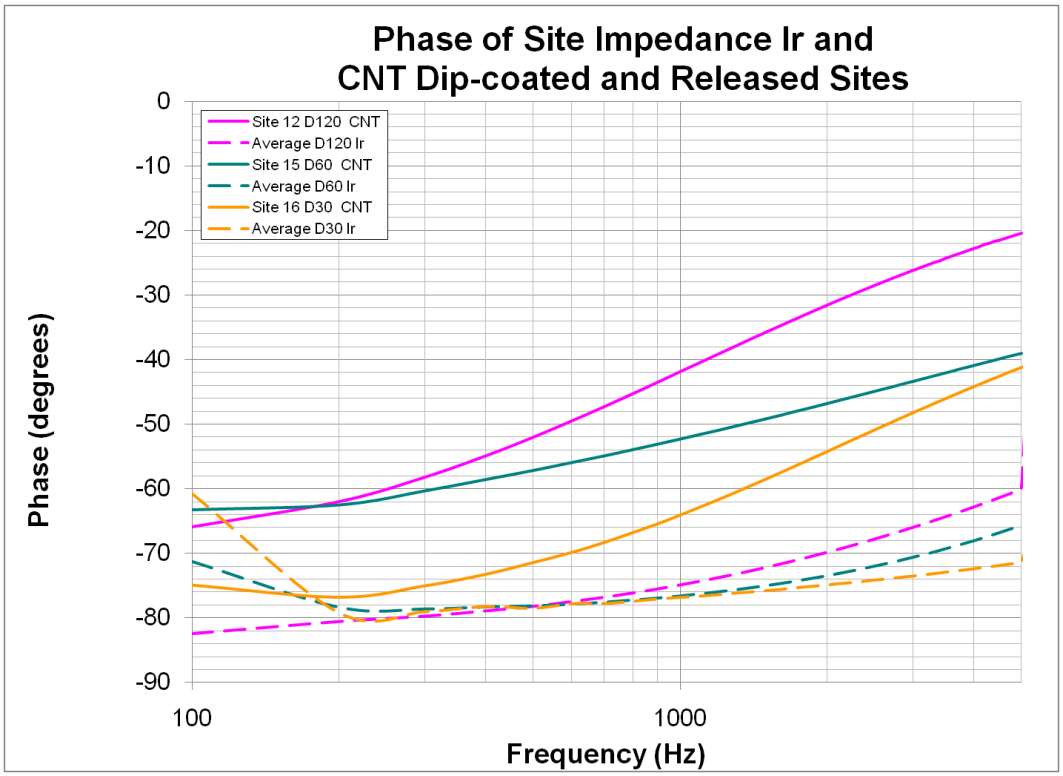




Fig. 3.13: Measured impedances of best CNT dip-coated sites (solid) on released probes in comparison to averages of good iridium sites (dashed). The legends indicated the five site diameters, for example D15 has a 15μm diameter.

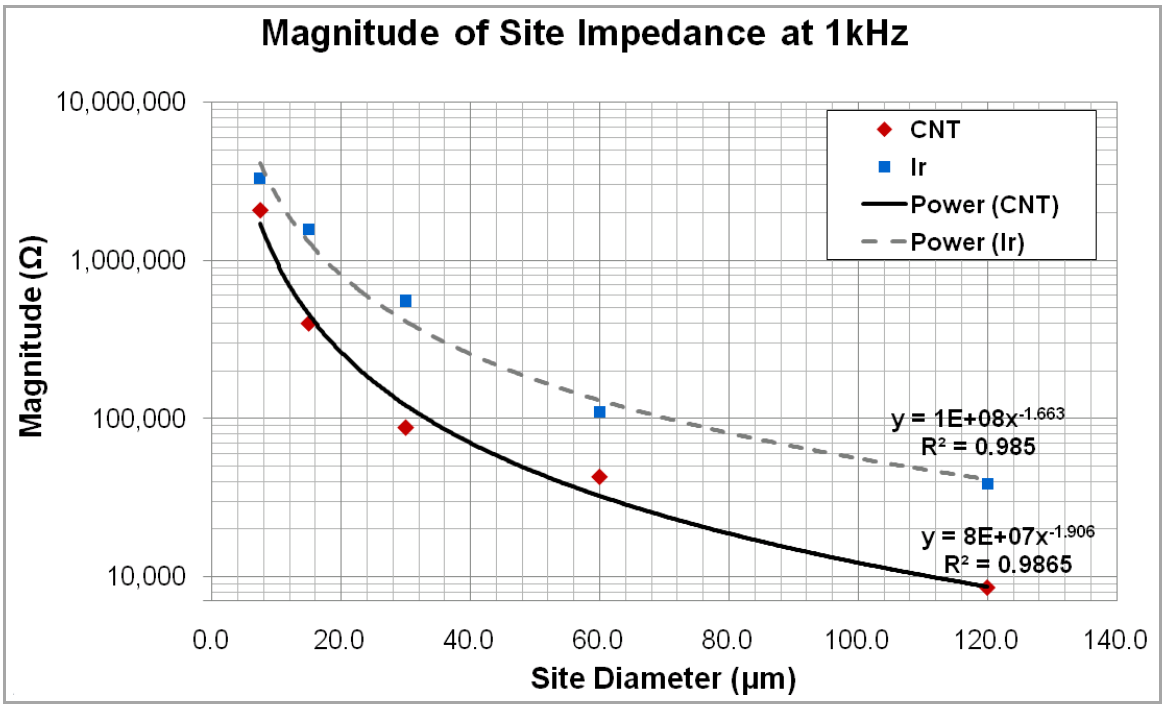



Fig. 3.14: Graph of the 1kHz impedances from Fig. 3.13 by site size and material.

### 3.3.5 CNT Growth on Non-Released Probes

Carbon nanotube growth was successfully achieved on non-released probe die. These pieces went through the processing steps delineated in Table 3.1 including the front-side probe definition, back-side thinning, and chromium protection layer deposited and then removed. A mask set was specifically designed to study CNT incorporation; these probes include a variety of site sizes and catalyst geometries in order to study properties including growth structure, densification, and impedance. Fig. 3.16 through Fig. 3.22 show photographs and SEMs of as-grown CNT forests on iridium sites.

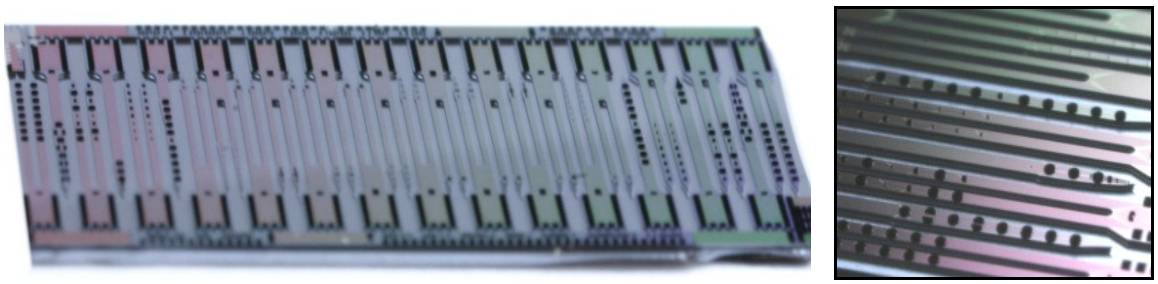


Fig. 3.15: Photographs of CNT growth (30sec) on non-released probes.

Fig. 3.16: Photograph of CNT growth (10min) on non-released probes. The taller forests clearly demonstrate the growth potential and have other applications including in work with *in vitro* cell cultures.

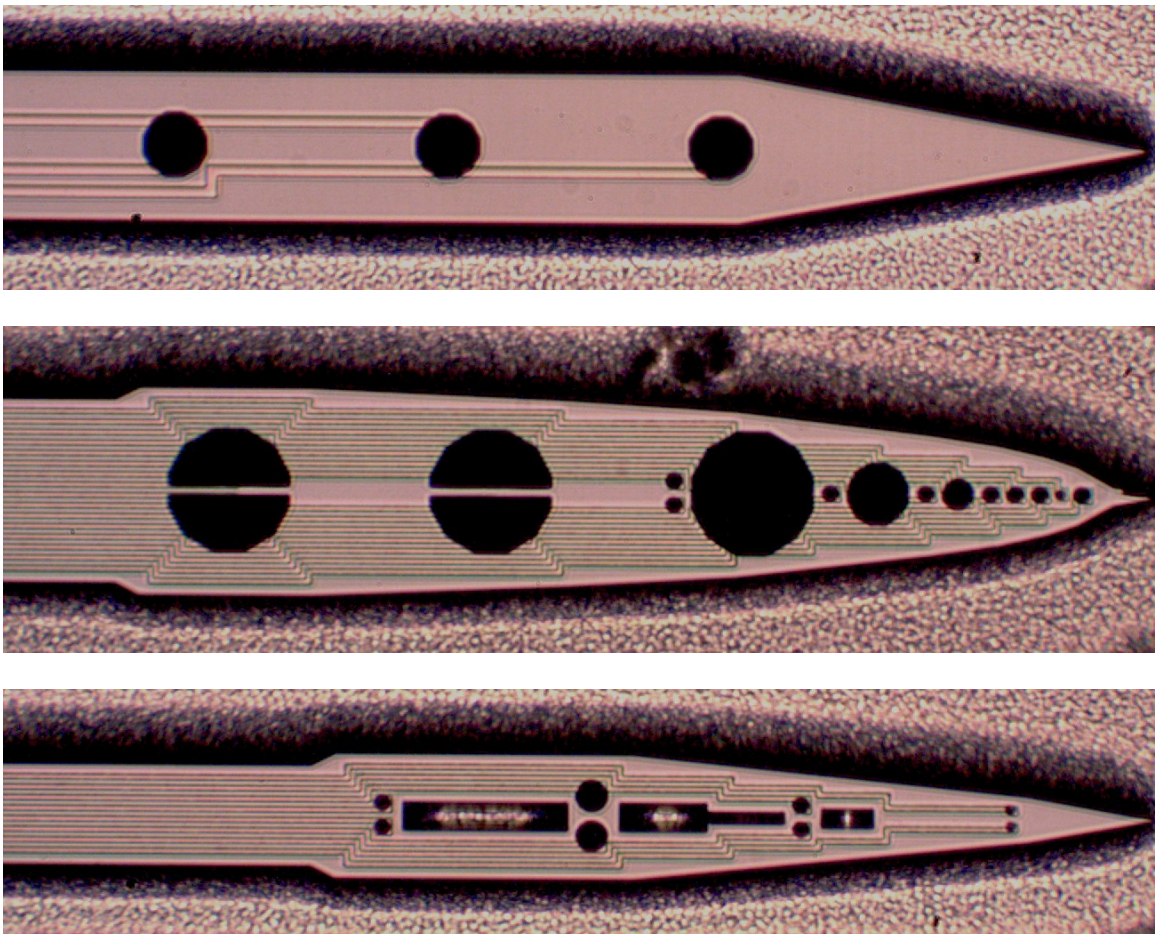


Fig. 3.17: CNT growth (30sec) on non-released probes showing sites on (top) probe with solid CNT patterns and (middle) probe with CNT patterned over iridium half circles (left) and several solid CNT site sizes alternating with 177μm$^2$ sites and (bottom) probe pairs of CNT patterned sites of 30, 15, and 7.5μm diameters.

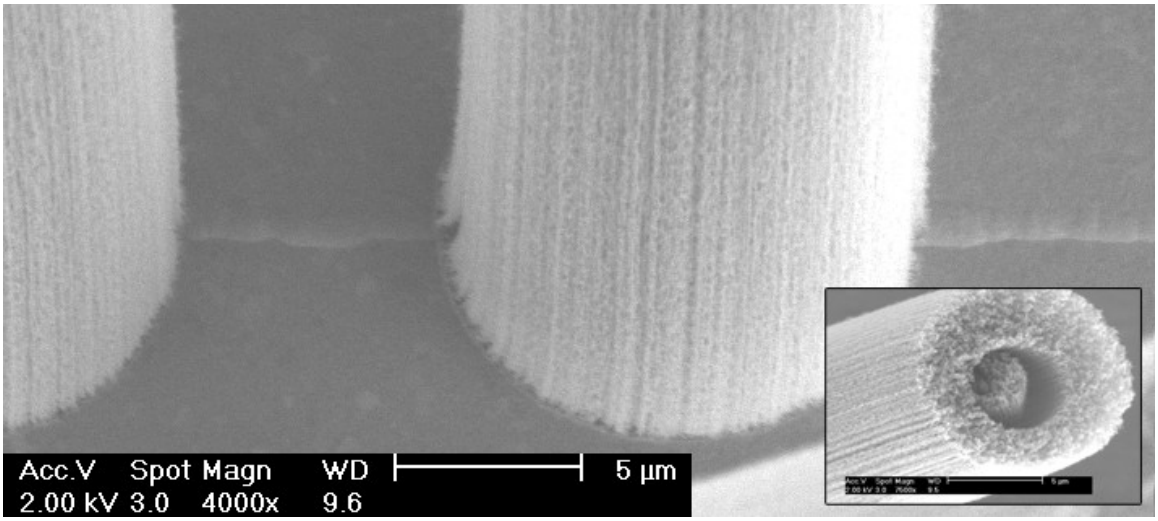



Fig. 3.18: SEM of CNT growth (2min) on a non-released probe showing small site diameter and vertical alignment of the tubes (images by M. Roberts).

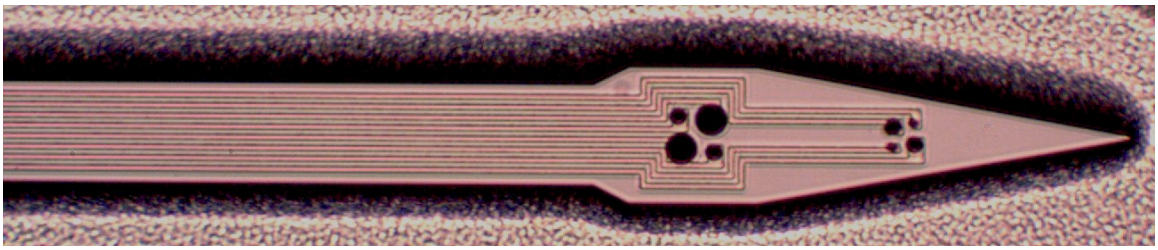


Fig. 3.19: CNT growth (30sec) on a recessed-site non-released probe with site arranged in tetrodes.

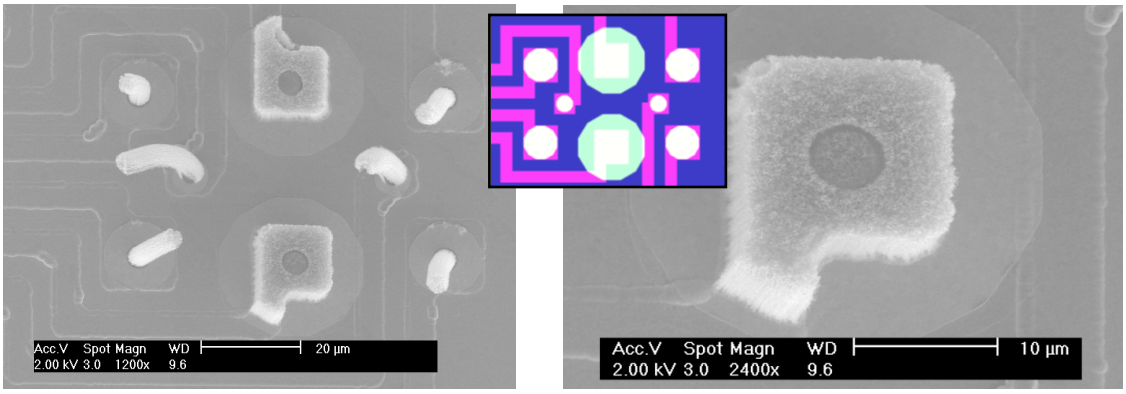



Fig. 3.20: SEM of CNT growth (1min) on a non-released probe (images by M. Roberts). The catalyst was originally patterned as the same size at the iridium site, but due to adhesion problems some lifted off before growth. Catalyst has highest viability in the recessed contacts as shown (left). The square site forest appears to be closer to the short height target (right). The inset shows the layout with the CNT catalyst locations (green/white).

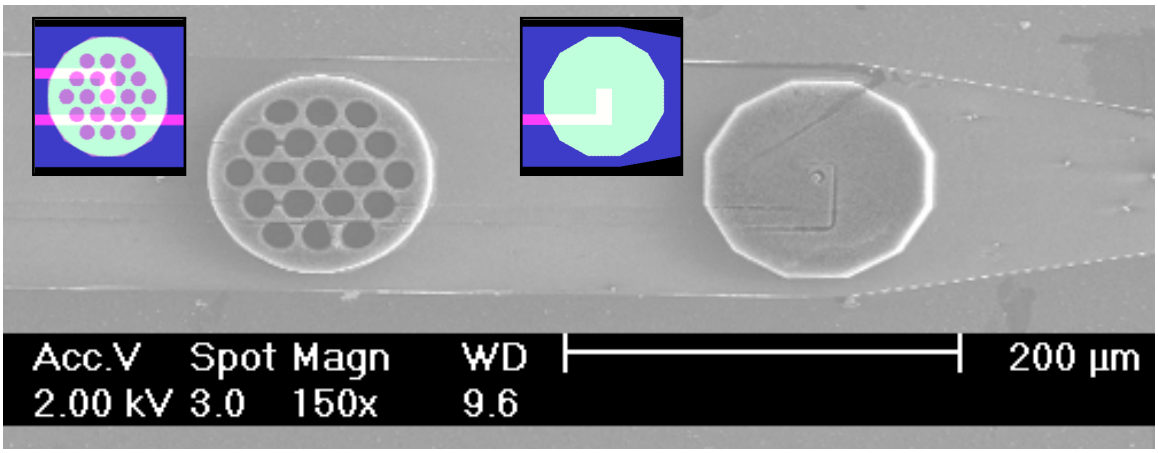



Fig. 3.21: SEM of CNT growth (45sec) on a non-released probe showing large diameter sites with sponge and solid CNT patterns (image by M. Roberts). The insets show close-ups of the layout with iridium (purple) and CNT catalyst (green/white) locations.

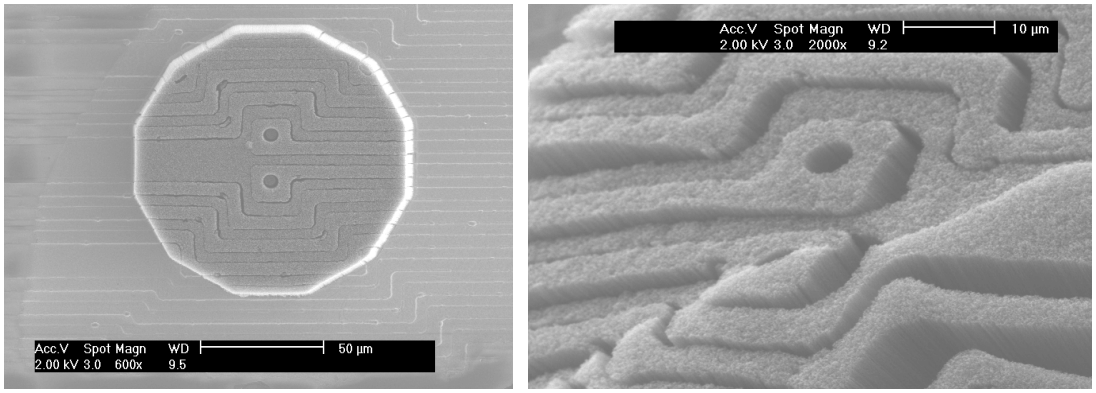



Fig. 3.22: SEM of CNT growth (45sec left and 2min right) on non-released probes showing the step height at the base is replicated at the top of the forest (images by M. Roberts).

### 3.3.6 CNT Growth on EDP Released Probes

Challenges were encountered with the growth of CNTs on released probes. These problems appear to be due to poor CNT catalyst adhesion. Another issue is the peeling of the metal layers after the high-temperature growth step. This occurs mainly where the lines are wide (backend and bond pads) which causes low yield although it does not affect every channel. In spite of these difficulties, Raman spectroscopy showed evidence of carbon at the center of an electrode site, as shown in Fig. 3.23. Further process development is needed to incorporate CNTs with the growth method.

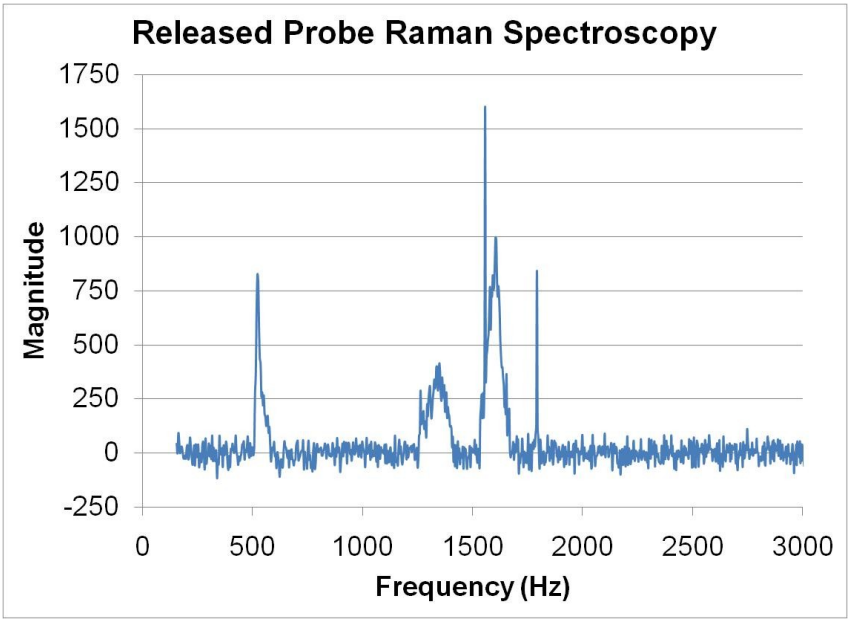



Fig. 3.23: Raman spectroscopy on a released probe after attempted CNT growth showing evidence of carbon present in the recessed contact.

### 3.4 Conclusions

Carbon nanotubes have been incorporated on iridium sites of non-released probes with two methods: dip-coating and *in situ* growth. Directions for incorporation on released probes have also been explored. Dip-coating has shown a decrease in site impedance on non-released probes of about one order of magnitude from that of iridium sites. The effect of adding the CNTs with this method is similar to increasing the parallel electrode capacitor in Randles model of the electrode-electrolyte interface. These steps in electrode development of CNT incorporation present an innovative opportunity to address fundamental yet unresolved issues of the electrode-tissue interface. However, significant work is still required before the value of CNTs is fully explored.

The dip-coating method enables CNT incorporation without major process modification and while retaining integrated polymer cables. However, with the growth-method of incorporation, integrated polymer cables can not be used due to the high-temperature of the growth step. There is potential for overcoming the CNT catalyst adhesion problem by performing the front-side etches before catalyst patterning to avoid exposing it to solvents. Creating recessed sites or adding other adhesion layers may also assist in overcoming this challenge. Using SOI (silicon-on-oxide) wafers with a DRIE

release would avoid the wet release but it would also prevent the standard integrated cable method.

Once a process flow for CNT incorporation on released devices is fully established, in vitro and in vivo tests should be performed to evaluate CNT stability over time (both shelf-life and accelerated saline soak tests) and the impact of CNTs on the immune reaction and recording lifetime.

# CHAPTER IV

# NEURAL RECORDING AMPLIFIER

In chronic prosthetic applications, or anytime additional circuitry is employed beyond the typical equipment found in a neuroscience recording booth, a recording amplifier located in close proximity to the electrode sites is advantageous to buffer the signal measured at this high impedance node. The need for a low-power low-area amplifier design is felt more keenly in high channel count systems. One such neural interface has been conceptually designed and is described in detail in Appendix A. This fully wireless 32-channel system with simultaneous recording and stimulation capabilities is intended for a 256-site 3-D electrode array in order to support neuroscience mapping studies. Further details on the front-end circuit and array are presented in Appendix B. The analog amplifier is the most critical front-end circuit component as it is instantiated thirty-two times, consumes static power, and has a design complexity that exceeds that of the analog current sources and multiplexers. This chapter presents the design and test of a neural recording amplifier, focusing on size and power consumption for use in the recording bank of this wireless implantable system.

## 4.1 Previous Neural Recording Amplifiers

Previous researchers have investigated methods for achieving DC input-stabilized low-noise low-power neural amplifiers with or without a tunable lower cutoff frequency [9, 57, 59, 107-109]. The most recent neural amplifier work at Michigan was done by Perlin [59]. To achieve a gain of 1000, her topology required an input capacitor of 50pF which dominated the total layout area (about $0.062mm^2$ of $0.098mm^2$). The challenge posed when decreasing the absolute value of the capacitors is that the value of the feedback capacitor nears that of parasitic capacitances present in the circuit.

### 4.2 A Dual-Stage 60dB Neural Recording Amplifier

In order to prevent amplifier saturation, one method of rejecting the DC component of the electrode site voltage is to utilize an AC-coupled topology. With the addition of a feedback capacitor, the input capacitor can also be used to set the closed-loop amplifier gain as the input-to-feedback capacitor ratio. However, for high gain applications, a single-stage design demands a large capacitor ratio [59]. Thus, such a design tends to require significant die space, especially since capacitor areas do not scale directly with transistor dimensions as the minimum feature size decreases. This quandary can be met by using two gain stages in series in order to achieve the total desired gain while alleviating the large capacitor ratio requirement. Thus, the input capacitor area can be reduced from that in a single-stage topology while maintaining a feedback capacitor value which is significantly above that of the parasitics. This concept was implemented in a 60dB (1000x) dual-stage design, as illustrated in Fig. 4.1, with a gain of 40dB (100x) for the first stage and 20dB (10x) for the second stage. The challenge in this scenario is to keep the circuit power low while supporting both stages with the necessary current. The engineering decisions included designing for a 0.5µm CMOS process with dual supplies (±1.5V) and ground provided to the circuit.

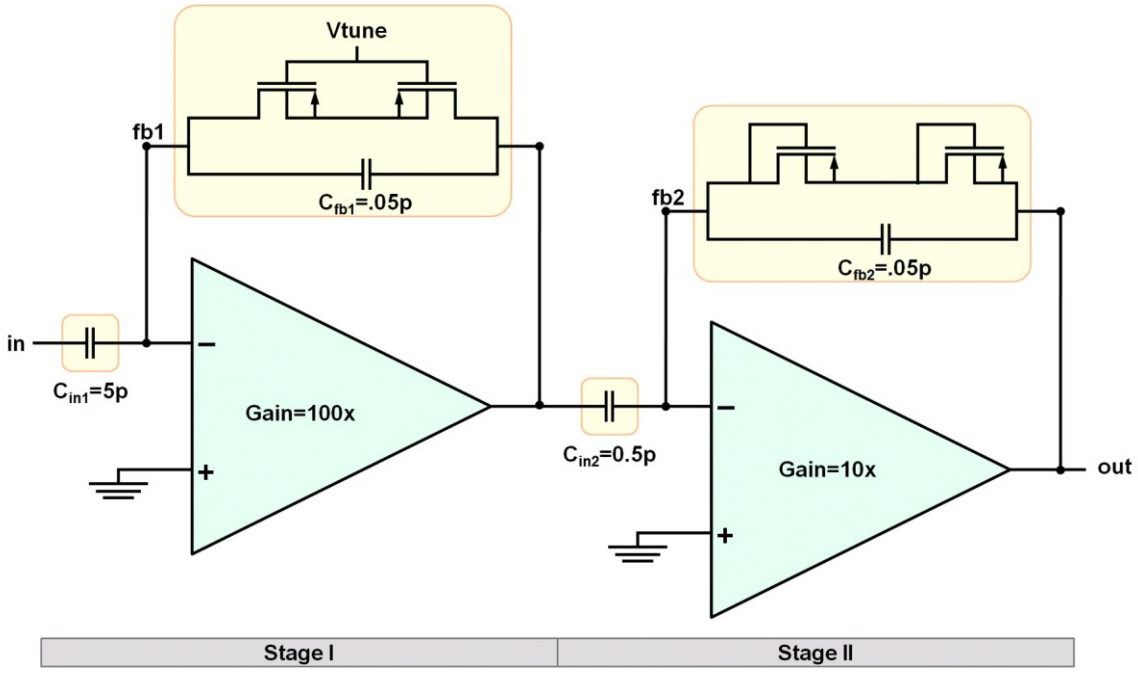



Fig. 4.1: Dual-stage topology for the 60dB neural recording amplifier.

### 4.2.1 Schematic Design

In addition to setting the desired gain, establishing the bandwidth required to amplify neural signals while rejecting out-of-band signals is important. The addition of a resistor in parallel with the feedback capacitor can be used to set the low cutoff frequency as $f_{lc}=1/(2\pi RC_{fb})$ [57]. A series of two diode-connected PMOS transistors, biased in the sub-threshold region, may be used as MOS-resistors (MOS-R); this is an effective means for achieving the large resistance required for the low cutoff frequency in a small area [57]. A tunable cutoff frequency enables the user to accept low-frequency field potentials when pertinent or to reject them if focusing on single-unit recordings. As previous designers have shown, the bandwidth of the amplifier can be tuned by adjusting the gate voltages of the (first set of) feedback MOS-R in order to control their effective resistance, and thus the low cutoff frequency [57, 59]. The known challenges with this approach are that process variations can cause large changes in the effective resistance of the MOS-R and that relatively small changes in tuning voltage can cause significant shifts in the cutoff frequency. The placement of the diode connected gates of the feedback MOS-R for the second stage and the substrate connections for the MOS-R of both stages were simulated before settling on the final schematic.

For design simplicity, the stage I and stage II open-loop amplifiers both employ the same topology, with a differential gain input sub-stage followed by an output sub-stage, as shown in Fig. 4.2 and Fig. 4.3. Since this topology uses relatively few transistors, the layout can take less area than many other designs. This is an important consideration since size is a critical factor for implantable circuits. Design, layout, simulations, and associated comments included herein rely extensively on [57, 108, 110, 111].

A Miller capacitor in series with a nulling resistor is connected across each second sub-stage in order to provide the frequency compensation necessary to ensure stability; this also sets the upper cutoff frequency of the amplifier [9, 57]. A diode-connected bias string (MN8, MP9) is used to supply the bias voltage to set the bias currents in the input sub-stage of both stage I and II. The bias string is shared not only by the two stages, but by all the amplifiers in the amplifier bank, which helps to achieve the low-power goal of the design.

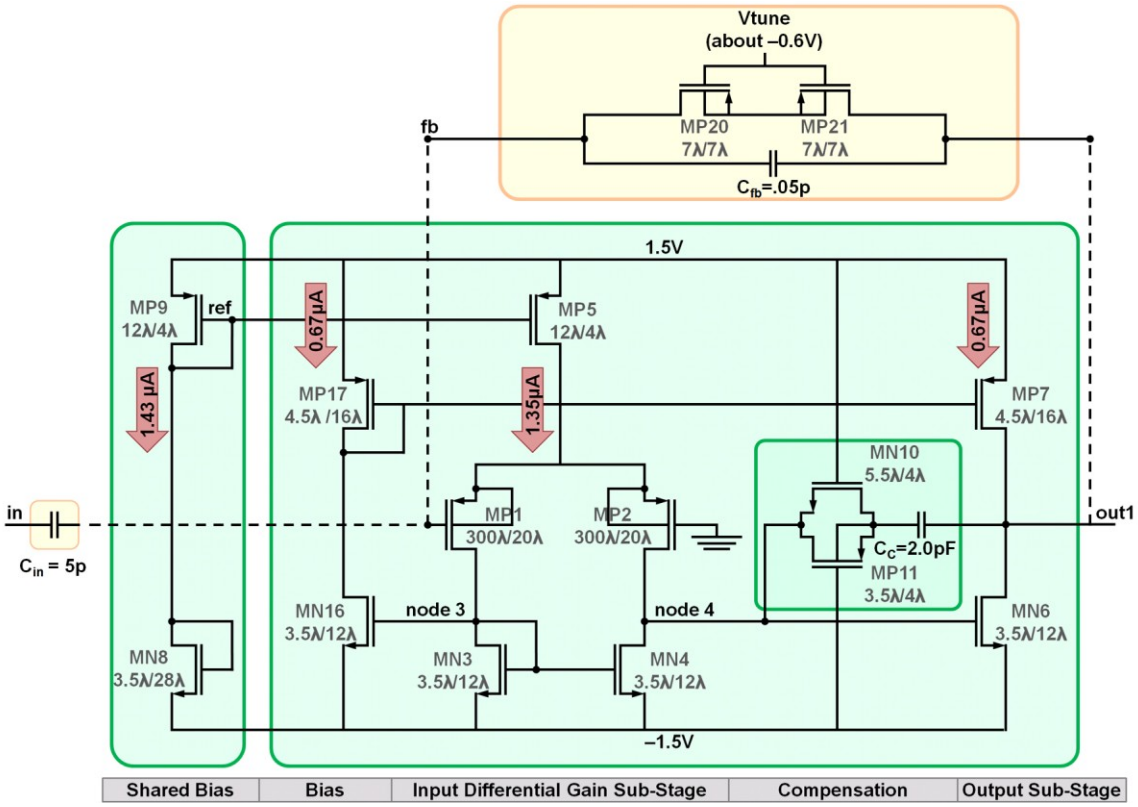



Fig. 4.2: Stage I (40dB) of the 60dB dual-stage amplifier. Lambda (λ) is 0.3µm.

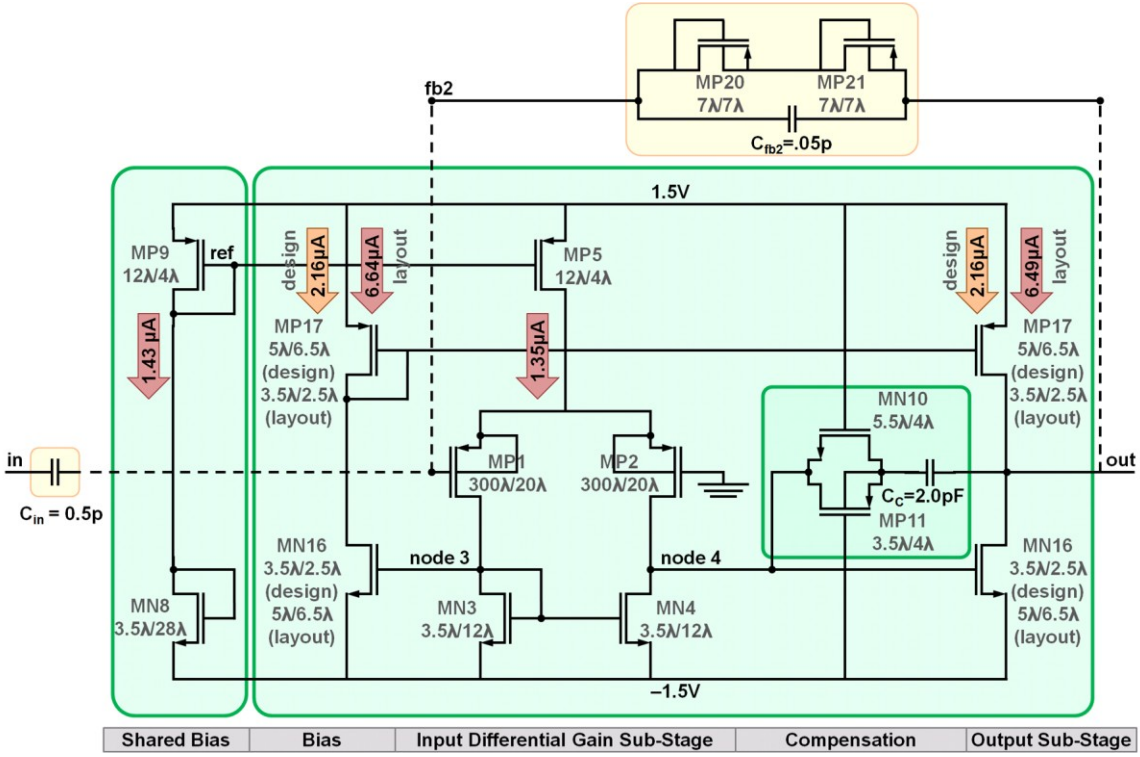



Fig. 4.3: Stage II (20dB) of the dual-stage amplifier. Lambda (λ) is 0.3µm. Accidental size switch in layout caused currents in two branches to increase.

The differential gain sub-stage consists of a PMOS-input differential pair (MP1, MP2) with a current mirror load (MN3, MN4). The transistors are matched so the source-coupled input transistors have the same device dimensions and drain-to-source saturation voltages and so the current mirror load transistors have the same dimensions and saturation voltages. The transistor values of this sub-stage are identical for stage I and II. As shown in Table 4.1, large gate-area PMOS input transistors are used in order to minimize Flicker (1/f) noise [108]. The transistors are sized so that the W/L ratios of other transistors are significantly smaller than the W/L of the input transistors to ensure the input transistors are the dominant source of thermal noise [108]. The bias current through the differential pair is set by MP5 mirroring the current through the bias string. The current mirror load performs the double-to-singled-ended conversion.

**Table 4.1: Transistor Dimensions**

| Role | Tx | Stage | Width | | Length | | W/L | W*L |
|---|---|---|---|---|---|---|---|---|
| **Input Sub-Stage** | MP1 | I & II | 300λ | 90µm | 20λ | 6µm | 7.50 | 540.00µm$^2$ |
| | MP2 | I & II | 300λ | 90µm | 20λ | 6µm | 7.50 | 540.00µm$^2$ |
| | MN3 | I & II | 3.5λ | 1.05µm | 12λ | 3.6µm | 0.29 | 3.78µm$^2$ |
| | MN4 | I & II | 3.5λ | 1.05µm | 12λ | 3.6µm | 0.29 | 3.78µm$^2$ |
| | MP5 | I & II | 12λ | 3.6µm | 4λ | 1.2µm | 3.00 | 4.32µm$^2$ |
| **Shared Bias** | MN8 | Bank | 3.5λ | 1.05µm | 28λ | 8.4µm | 0.13 | 8.82µm$^2$ |
| | MP9 | Bank | 12λ | 3.6µm | 4λ | 1.2µm | 3.00 | 4.32µm$^2$ |
| **Output Sub-Stage** | MN6 | I | 3.5λ | 1.05µm | 12λ | 3.6µm | 0.29 | 3.78µm$^2$ |
| | | II | 5λ | 1.5µm | 6.5λ | 1.95µm | 0.77 | 2.93µm$^2$ |
| | MP7 | I | 4.5λ | 1.35µm | 16λ | 4.8µm | 0.28 | 6.48µm$^2$ |
| | | II | 3.5λ | 1.05µm | 2.5λ | 0.75µm | 1.40 | 0.79µm$^2$ |
| **Bias** | MN16 | I | 3.5λ | 1.05µm | 12λ | 3.6µm | 0.29 | 3.78µm$^2$ |
| | | II | 5λ | 1.5µm | 6.5λ | 1.95µm | 0.77 | 2.93µm$^2$ |
| | MP17 | I | 4.5λ | 1.35µm | 16λ | 4.8µm | 0.28 | 6.48µm$^2$ |
| | | II | 3.5λ | 1.05µm | 2.5λ | 0.75µm | 1.40 | 0.79µm$^2$ |
| **Compensation** | MN10 | I & II | 5.5λ | 1.65µm | 4λ | 1.2µm | 1.38 | 1.98µm$^2$ |
| | MP11 | I & II | 3.5λ | 1.05µm | 4λ | 1.2µm | 0.88 | 1.26µm$^2$ |
| **Feedback** | MP20 | I & II | 7λ | 2.1µm | 7λ | 2.1µm | 1.00 | 4.41µm$^2$ |
| | MP21 | I & II | 7λ | 2.1µm | 7λ | 2.1µm | 1.00 | 4.41µm$^2$ |

The output sub-stage is a common source NMOS transistor (MN6) with a PMOS load (MP7). A biasing scheme is employed for this sub-stage in which another string of matched transistors (MN16, MP17) are used. The gate of MN16 is controlled by the node (node 3) opposite the first sub-stage output (node 4) and a current mirror is formed between MP7 and MP17. The output sub-stage allows for a large output swing, especially with the design values for stage II. The W/L ratios of the transistors in the output sub-stage of stage II are larger than those of stage I and the bias current for this branch is designed larger than the corresponding stage I branch so that the complete two-stage amplifier can drive the necessary interconnect and other parasitic capacitances.

### 4.2.2 Two-Stage Amplifier Layout

Mentor Graphics IC Station was used for the two-stage amplifier layout, which is presented in Fig. 4.4. Throughout the layout, symmetry was employed whenever possible to assist with device matching, reduce common-mode noise, and diminish even-order nonlinearity [111]. As the first transistors in the signal path, the differential pair comprises the most critical devices. A common-centroid layout surrounded by guard rings was used to cancel first-order gradients and isolate the devices [111]. The most accurate method of creating capacitor ratios is to use unit capacitors. However, this approach takes more space than regular capacitors. For *in vivo* amplification, size is a more critical parameter than precise gain; therefore, unit capacitors were not used.

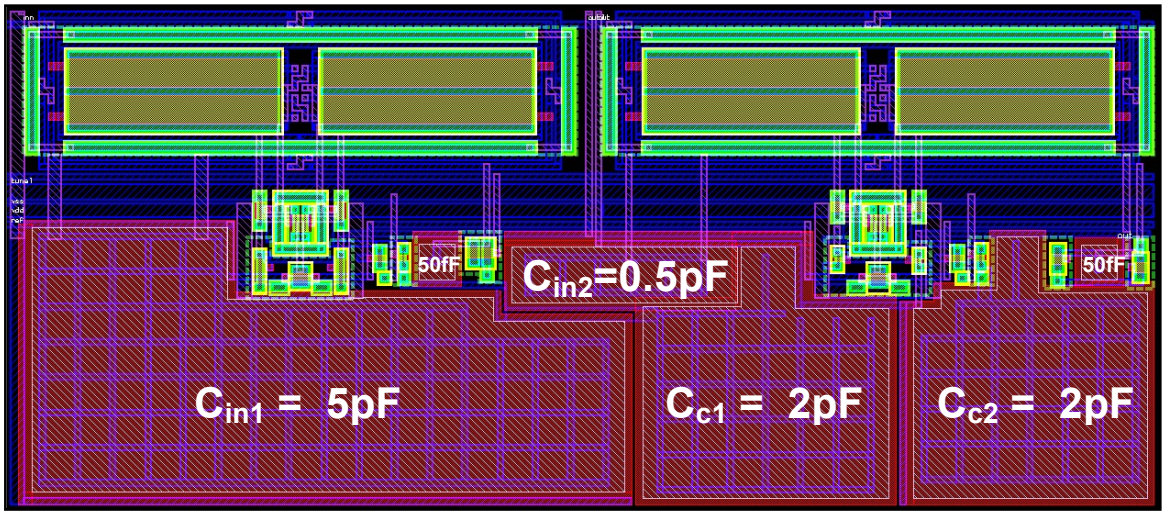



Fig. 4.4: Dual-stage 60dB amplifier layout in 0.0255mm$^2$ (243.45µm x 104.85µm) with a simulated power dissipation of 51.51µW, excluding the shared bias.

### 4.2.3 Post-Layout Simulations

The layout program, Mentor Graphics IC Station, was used for post-layout netlist extraction and HSPICE was employed to simulate the circuit. During layout, the sizes of two pairs of transistors were accidentally flipped in stage II, as shown in Fig. 4.3. While the amplifier still simulates the expected gain, this causes a significant increase in power consumption. In re-fabricating this amplifier, this mistake should be corrected. The following post-layout simulation results are based on the layout that was already fabricated, including this oversight, unless otherwise noted.

#### 4.2.3.1 Simulation Parameters and Process Corners

A model file supplies the simulation program with the transistor threshold voltages and other critical parameters. While the foundry seeks to control these parameters during fabrication, there may be deviations from the "typical" values. In order to assist designers in developing robust circuits which are capable of functioning over the expected possible range of device parameters, the MOSIS website provides five model files. These files are intended to represent the typical values and the four extremes, the process corners. The process corners are labeled based on the relative speed of NMOS devices followed by the speed of PMOS devices (fast-fast, slow-slow, fast-slow, slow-fast). The website also provides on-line test results from various fabrication runs. Threshold voltage is crucial to circuit performance. The NMOS and PMOS threshold voltages from the five model files are graphed in Fig. 4.5. Threshold values from on-line test data for five runs in 2006 are plotted on the same figure; these values fall near or within the quadrilateral defined by the process corners as expected. Values from ten recent (2008) runs were also included. Some of these values are significantly outside of the process corner quadrilateral. In order to more accurately represent process variations seen in recent fabrication runs, the threshold values for the fast-fast model file was updated as shown on the graph. The typical model file and all four corners, with the update, were used to simulate the post-layout circuit. Unless otherwise noted, the simulation results presented are based on the typical model file.

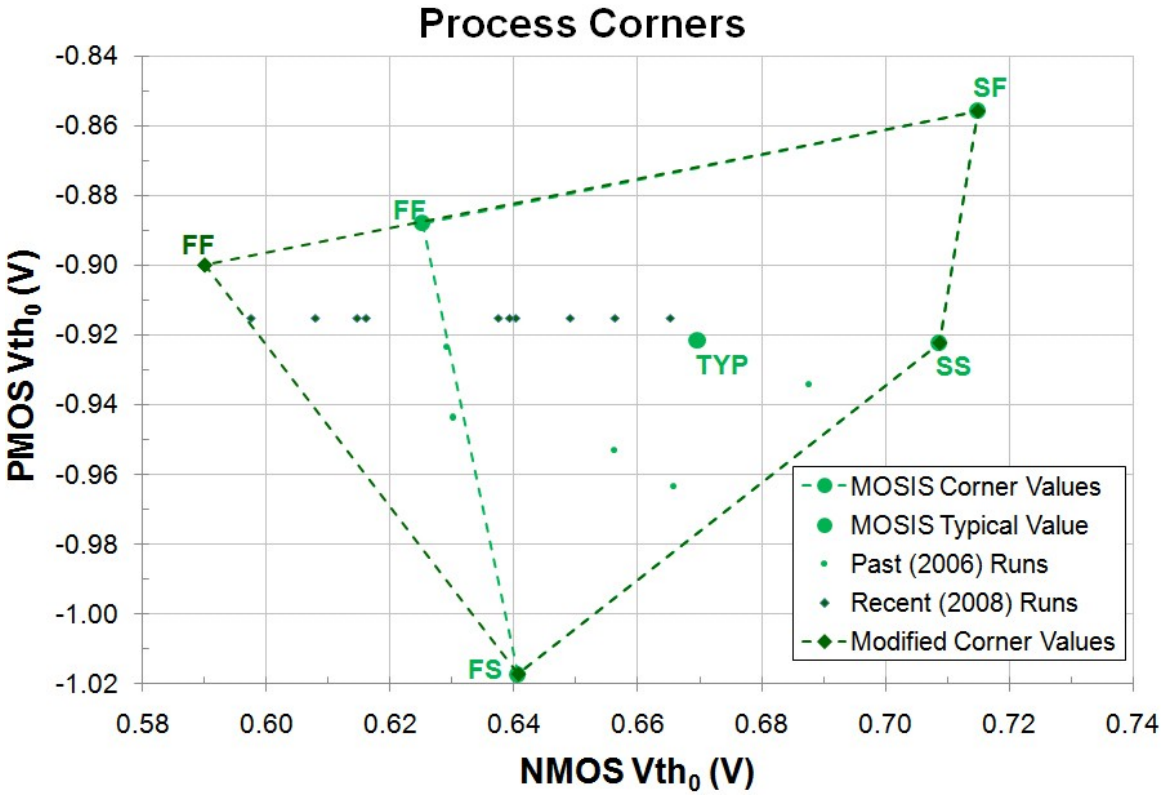



Fig. 4.5: Process corners based on the MOSIS on-line model files and test data. The corners are labeled based on the relative speed of NMOS devices followed by the speed of PMOS devices (fast-fast, slow-slow, fast-slow, slow-fast).

#### 4.2.3.2 Power Dissipation

Power dissipation is a crucial parameter for *in vivo* electronics in order to prevent tissue damage through overheating. In a fully implantable wireless system with a bank of amplifiers to buffer multiple recording channels, the need for a low power design becomes even more acute. The current through each branch was determined for the five model files and for the intended design as well as the actual fabricated transistor sizes (see above), as shown in Table 4.2. The corresponding power was calculated. Using the typical model file, the total power dissipation is simulated as 25.09µW and 51.51µW for the design and layout transistor dimensions, respectively. The doubled power between the intended and fabricated designs underscores the benefit that would result from re-fabricating with the intended device dimensions. These values do not include the bias string that supports the input sub-stage since it is used by all of the amplifiers in a bank. The value of 51.51µW dissipated power in the amplifier layout area corresponds to a power density of 2mW/mm$^2$.

| Table 4.2: Amplifier Power Dissipation | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Current (μA) | | | | | | Power (μW) | | |
| **Model File** | **Shared Bias (MP9)** | **Stage** | **Input Sub-Stage (MP5)** | **Output Sub-Stage (MP7)** | **Bias (MP17)** | **Total per Stage** | **Total per Stage** | **Total for Design Dimensions** | **Total for Layout Dimensions** |
| **Typical** | 1.43 | **I** | 1.35 | 0.67 | 0.67 | 2.69 | 8.07 | | |
| | | **IID** | 1.35 | 2.16 | 2.16 | 5.67 | 17.02 | **25.09** | |
| | | **IIL** | 1.35 | 6.49 | 6.64 | 14.48 | 43.44 | | **51.51** |
| **Fast-Fast** | 1.78 | **I** | 1.68 | 0.84 | 0.84 | 3.36 | 10.09 | | |
| | | **IID** | 1.68 | 1.41 | 1.40 | 4.49 | 13.46 | **23.56** | |
| | | **IIL** | 1.68 | 7.10 | 7.23 | 16.01 | 48.03 | | **58.12** |
| **Slow-Slow** | 1.35 | **I** | 1.27 | 0.64 | 0.64 | 2.54 | 7.63 | | |
| | | **IID** | 1.27 | 1.75 | 1.75 | 4.77 | 14.30 | **21.93** | |
| | | **IIL** | 1.27 | 6.18 | 6.32 | 13.78 | 41.34 | | **48.97** |
| **Fast-Slow** | 1.31 | **I** | 1.21 | 0.60 | 0.60 | 2.42 | 7.25 | | |
| | | **IID** | 1.21 | 1.55 | 1.56 | 4.32 | 12.97 | **20.21** | |
| | | **IIL** | 1.21 | 5.39 | 5.57 | 12.17 | 36.51 | | **43.75** |
| **Slow-Fast** | 1.70 | **I** | 1.63 | 0.81 | 0.81 | 3.25 | 9.75 | | |
| | | **IID** | 1.63 | 2.39 | 2.39 | 6.41 | 19.23 | **28.99** | |
| | | **IIL** | 1.63 | 6.72 | 6.84 | 15.19 | 45.56 | | **55.31** |
| IID values were simulated with the intended transistor dimensions for the second stage design and IIL values were simulated with the transistor dimensions used in layout (see text). Total values do not include the shared bias. | | | | | | | | | |

#### 4.2.3.3 Stage I and Stage II Open-Loop Gain Phase Spectrum

In order to have a robust closed-loop amplifier design, the open-loop characteristics of the two stages must be investigated. The simulated frequency response for each stage was plotted for the design and the layout as shown in Fig. 4.6 and Fig. 4.7 respectively. High DC gain helps to ensure more ideal function of the operational amplifier in feedback configuration. The DC gain was estimated from the low frequency gain of the frequency response; both stages have an open-loop DC gain above 80dB.

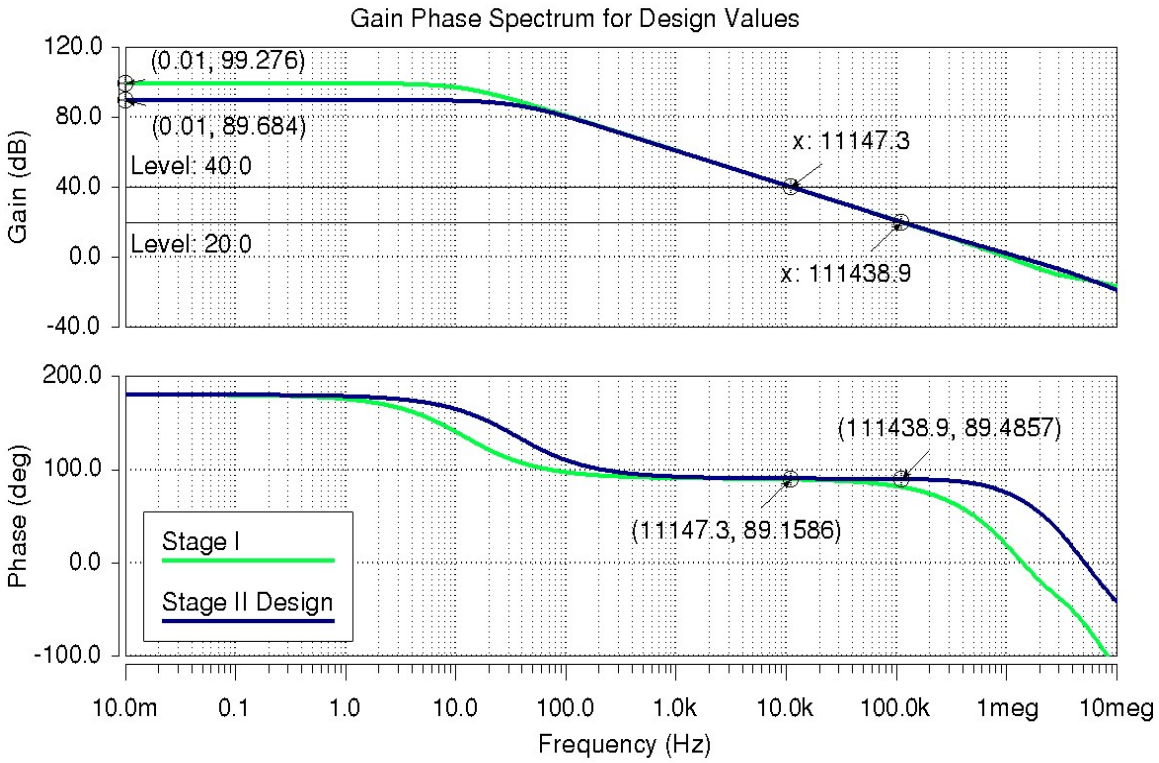



Fig. 4.6: The simulated open-loop gain phase spectrum for stage I (Cload = 0.5pF) and stage II (Cload = 5pF) using the design values for transistor dimensions.

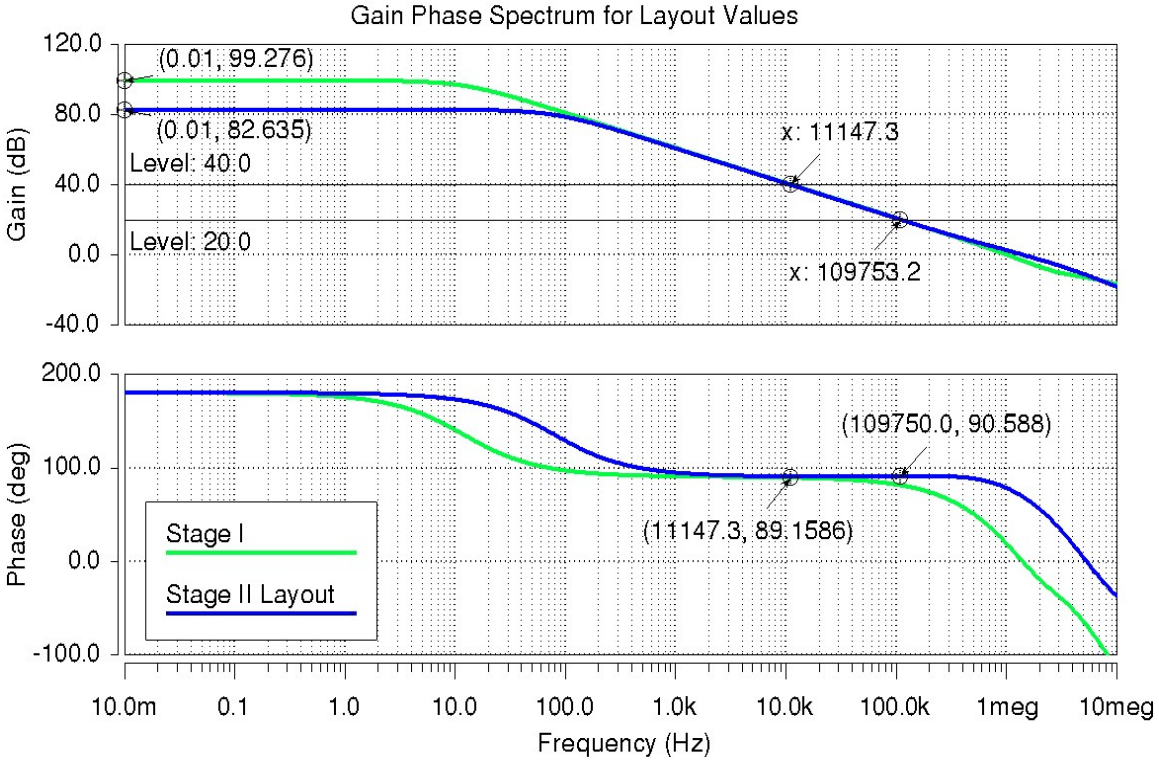



Fig. 4.7: The simulated open-loop gain phase spectrum for stage I (Cload = 0.5pF) and stage II (Cload = 5pF) using the layout values for transistor dimensions.

The load capacitance will affect the drop-off of the gain over frequency and the corresponding phase of the circuit. For these simulations, the load capacitor used for stage I was the layout-version of the closed-loop input capacitor for stage II. The load capacitor for stage II was supplied in HSPICE. The larger the phase margin of a circuit, the greater its stability. For closed-loop use, phase margin is gain specific. With feedback, stage I will operate at 40dB and stage II at 20dB; the associated frequencies and their corresponding phases were determined for these levels of gain. The phase margin is measured $180^{O}$ from the DC phase. With 0.5pF and 5.0pF of load capacitance for stage I and II respectively, the phase margin at their associated gains were both above $85^{O}$. Unless otherwise specified, these values of load capacitances were also used in other simulations of which results are presented. The load capacitor for stage II was also varied in HSPICE to see the effects of a span of capacitances (from 5pF to 50pF) in preparation for parasitic capacitances due to possible interconnects to an off-chip circuit; the corresponding gain phase spectrum is presented in Fig. 4.8.

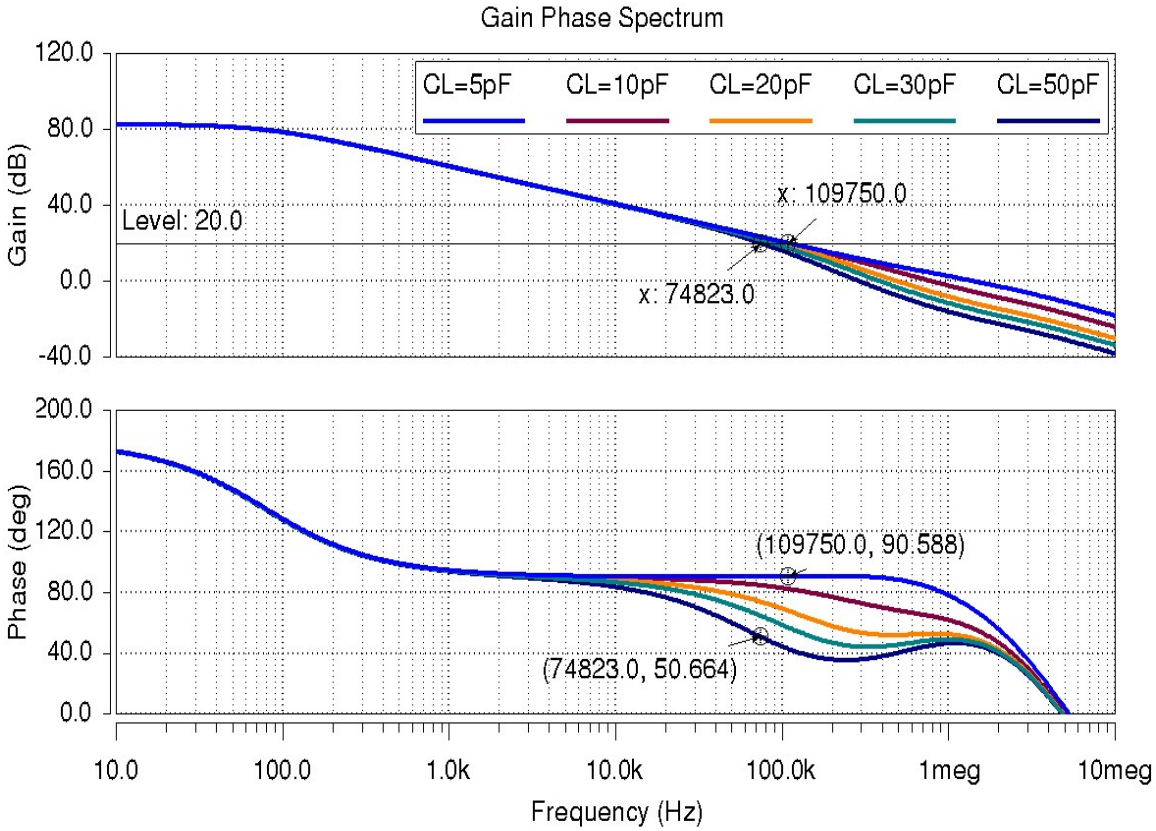



Fig. 4.8: Simulated effect of load capacitance on the phase margin of the stage II open-loop amplifier.

#### 4.2.3.4 Closed-Loop Frequency Response & Low Cutoff Frequency Tuning

The frequency response for the closed-loop stage I amplifier and the entire closed-loop circuit are presented in Fig. 4.9. The in-band gains of 40dB (stage I) and 59dB (stage I and stage II combined) are near the target values as are the lower (123Hz, Vtune = -0.6V) and upper (9.9kHz) cutoff frequencies for the complete amplifier. The low cutoff frequency is tunable by adjusting the voltage on the gate of the stage I feedback transistors as indicated in Table 4.3. The simulated frequency responses for a series of tuning voltages are plotted in Fig. 4.10 and the relationship between tuning voltage and the low cutoff frequency is graphed in Fig. 4.11.

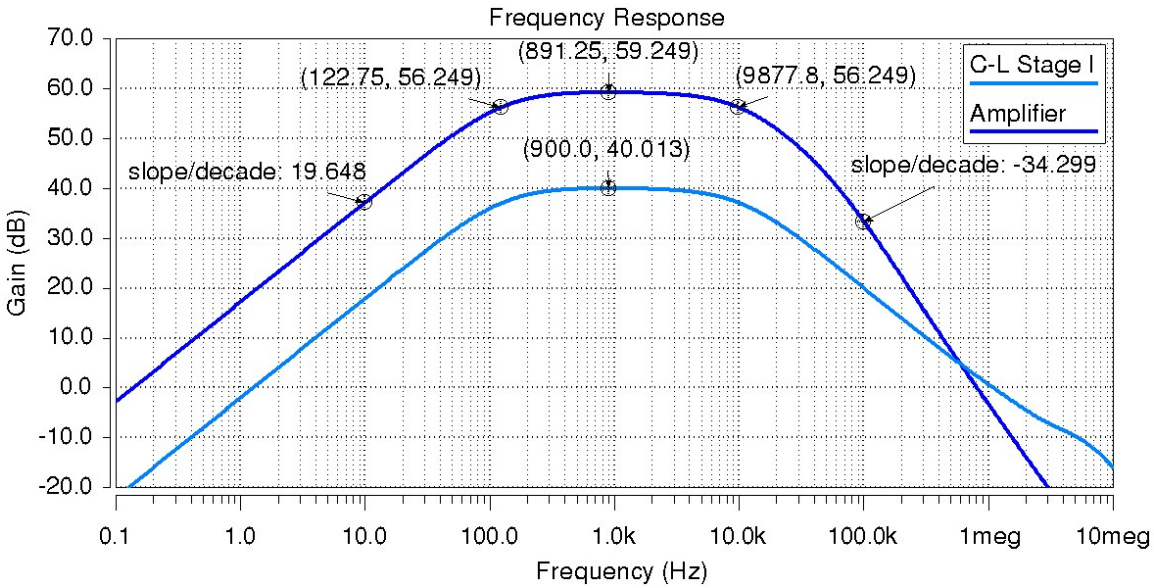



Fig. 4.9: Simulated post-layout frequency response for the two-stage amplifier showing the in-band gain, lower and upper cutoff frequencies, and roll-off.

**Table 4.3: Simulated Tuning of the Low-Cutoff Frequency**

| Tuning Voltage (V) | Maximum In-Band Gain (dB) | Low-Cutoff (-3dB) Frequency (Hz) | Upper-Cutoff (-3dB) Frequency (kHz) |
|---|---|---|---|
| 0.00 | 60.17 | --- | 7.70 |
| -0.45 | 59.21 | 2.44 | 9.89 |
| -0.50 | 59.21 | 9.02 | 9.89 |
| -0.55 | 59.22 | 33.36 | 9.87 |
| -0.60 | 59.25 | 122.75 | 9.88 |
| -0.65 | 59.28 | 440.34 | 10.11 |

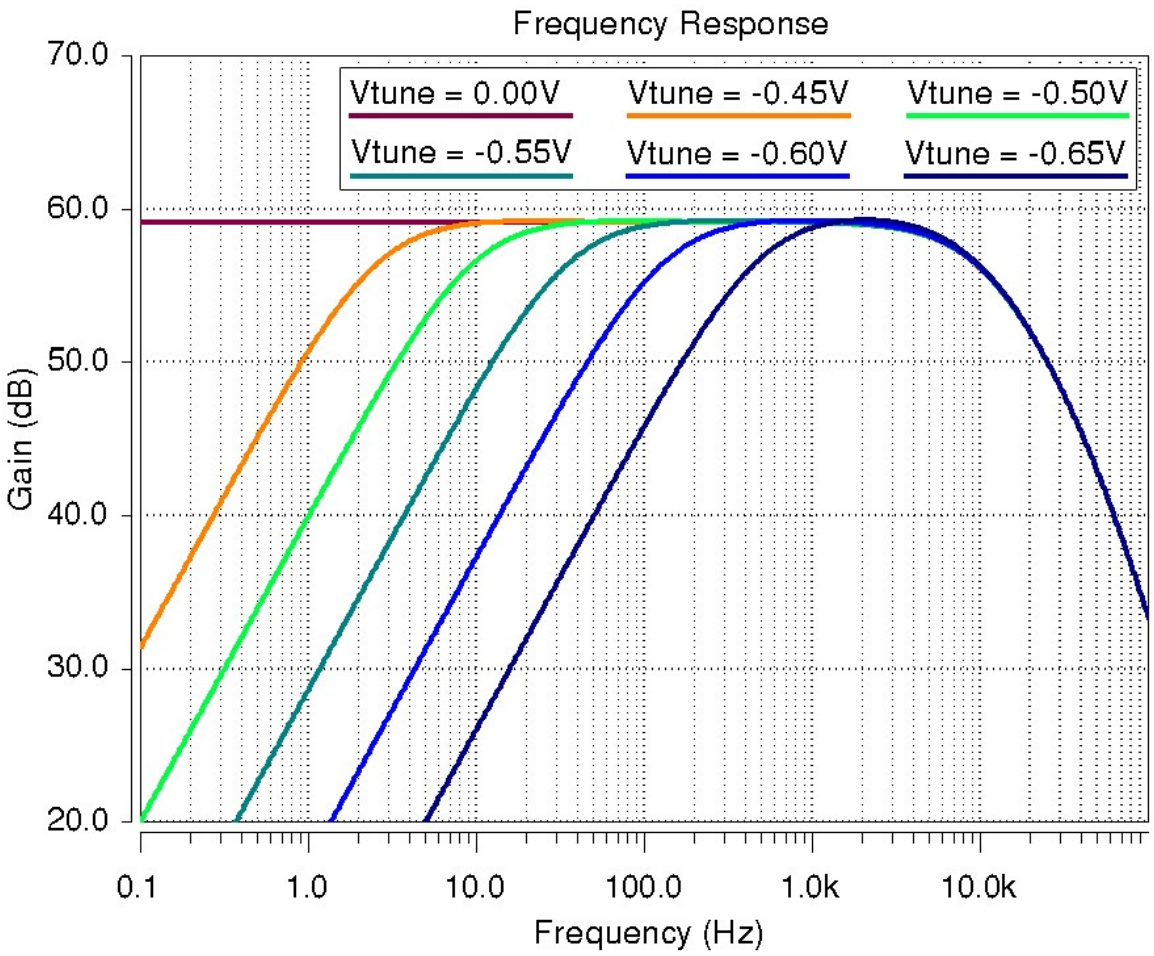



Fig. 4.10: Simulated effect of varying the tuning voltage on the frequency response for the two-stage amplifier.

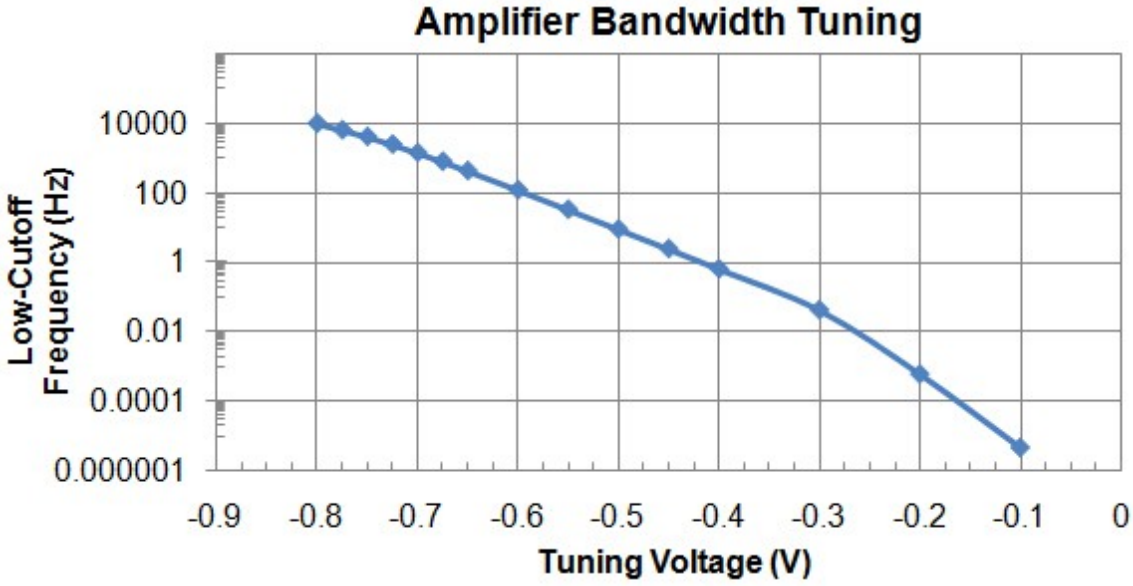



Fig. 4.11: Plot of low cutoff frequency as a function of tuning voltage from simulations.

In systems designated for recording action potentials of individual neurons, the low cutoff frequency could be set above the frequencies of field potentials and of 60Hz noise yet below that of typical neural signals. In practice, without tunability, this can be difficult due to the large variations from run to run in the effective resistance of the feedback transistors due to process variations. This point is emphasized by examining the simulated low cutoff frequency for a given tuning voltage while altering the model file. The simulated frequency responses for the five model files are graphed in Fig. 4.12. The gain and upper-cutoff frequency remain about the same from model file to model file. However, the lower cutoff frequency varies by more than 800Hz, from about 2Hz for the fast-NMOS/slow-PMOS case to around 820Hz for the slow-NMOS/fast-PMOS case. The other question that arises is whether or not a common tuning voltage is practical for all channels. This is addressed further in the test results section.

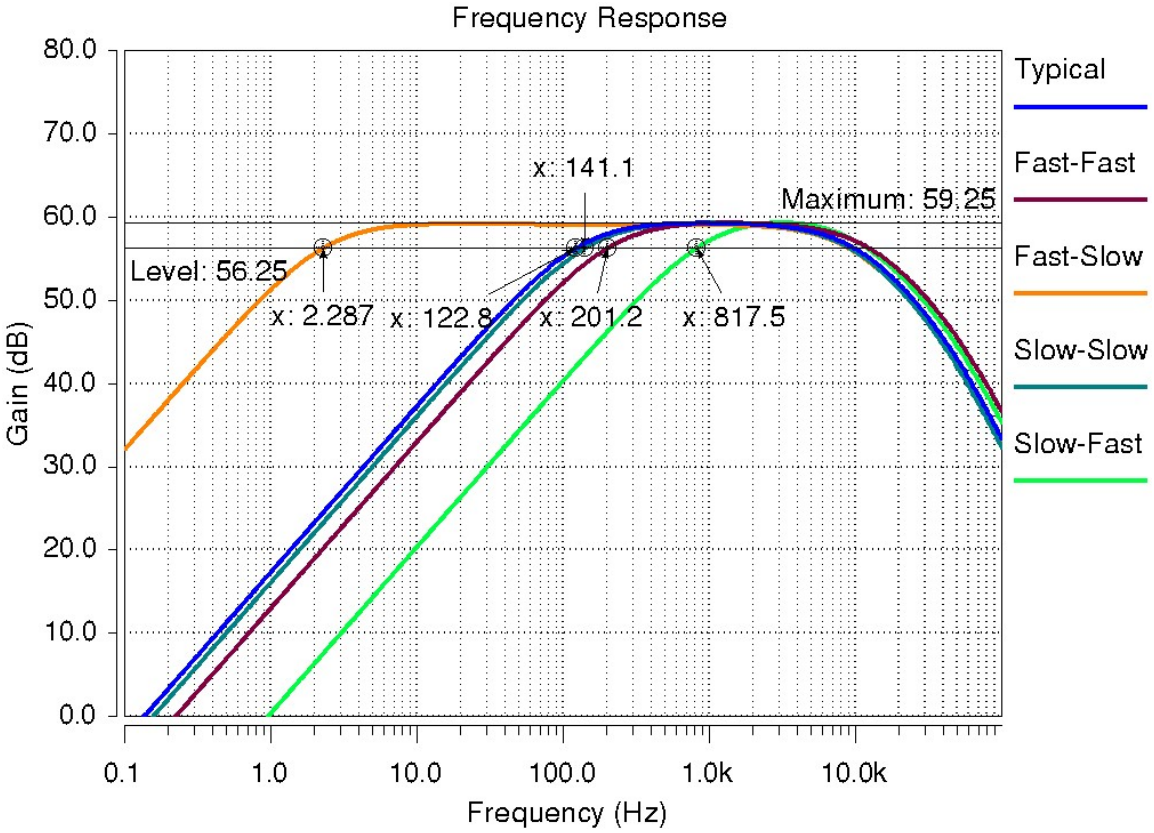



Fig. 4.12: Effect of varying the transistor model file on the simulated frequency response of the amplifier. The tuning voltage is -0.6V. The speed designations are written in NMOS-PMOS order. The lower cutoff frequencies are indicated using the maximum in-band gain of the typical model file as the reference.

#### 4.2.3.5 Common Mode Rejection Ratio

Common mode noise appears on both inputs of a differential gain stage. The common mode rejection ratio (CMRR) for the stage I and stage II amplifiers was simulated using a negative feedback topology with a common mode source in the feedback loop and an identical common mode source at the positive input. The frequency response of $(V_{out}/V_{cm})^{-1}$ was plotted as shown in Fig. 4.13. For each stage, the CMRR was above 100dB and 95dB at low and 1kHz frequencies respectively.

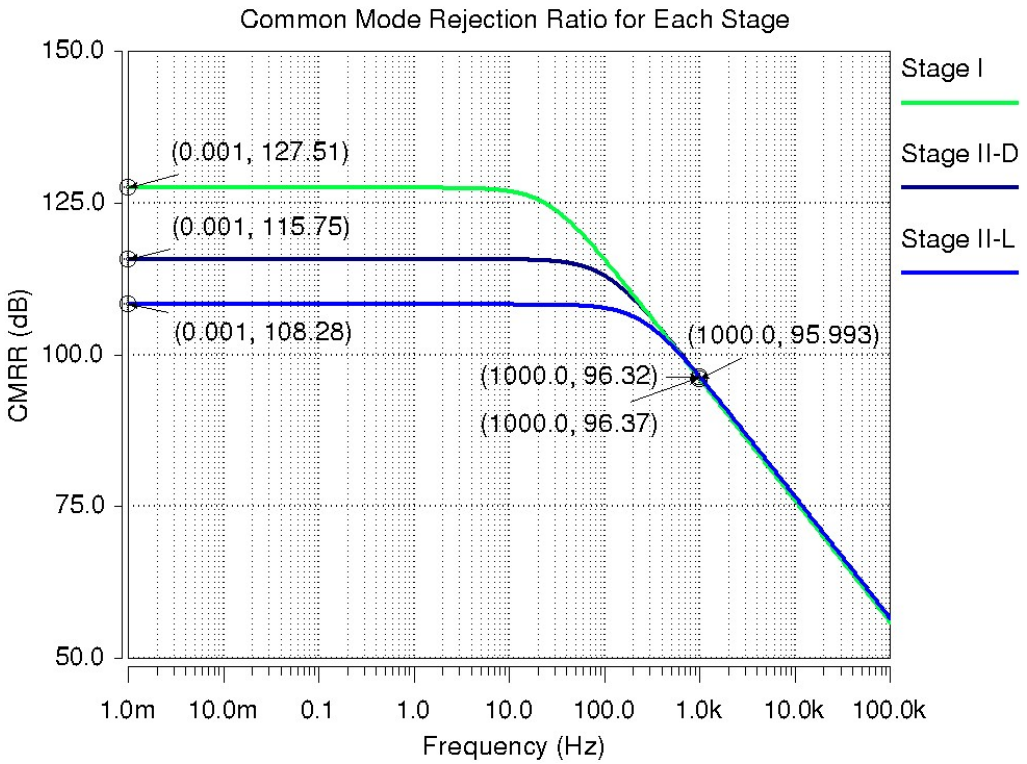



Fig. 4.13: Simulated common mode rejection ration (CMRR) for stage I and stage II using transistor design (D) and layout (L) values.

#### 4.2.3.6 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) reflects the amount an amplifier rejects noise on the power supply lines. This is especially important for analog circuits which are on the same substrate as digital circuits. The PSRR of each stage was simulated using a unity-gain feedback configuration and $(V_{out}/V_{supply})^{-1}$ was plotted versus frequency as presented in Fig. 4.14; the PSRR was above 85dB and 60dB at low and 1kHz frequencies respectively. The PSRR for the two-stage amplifier with feedback was also simulated; Fig. 4.15 shows the resulting graph of $(V_{out}/V_{supply})^{-1}/(\text{Gain Spectrum})^{-1}$.

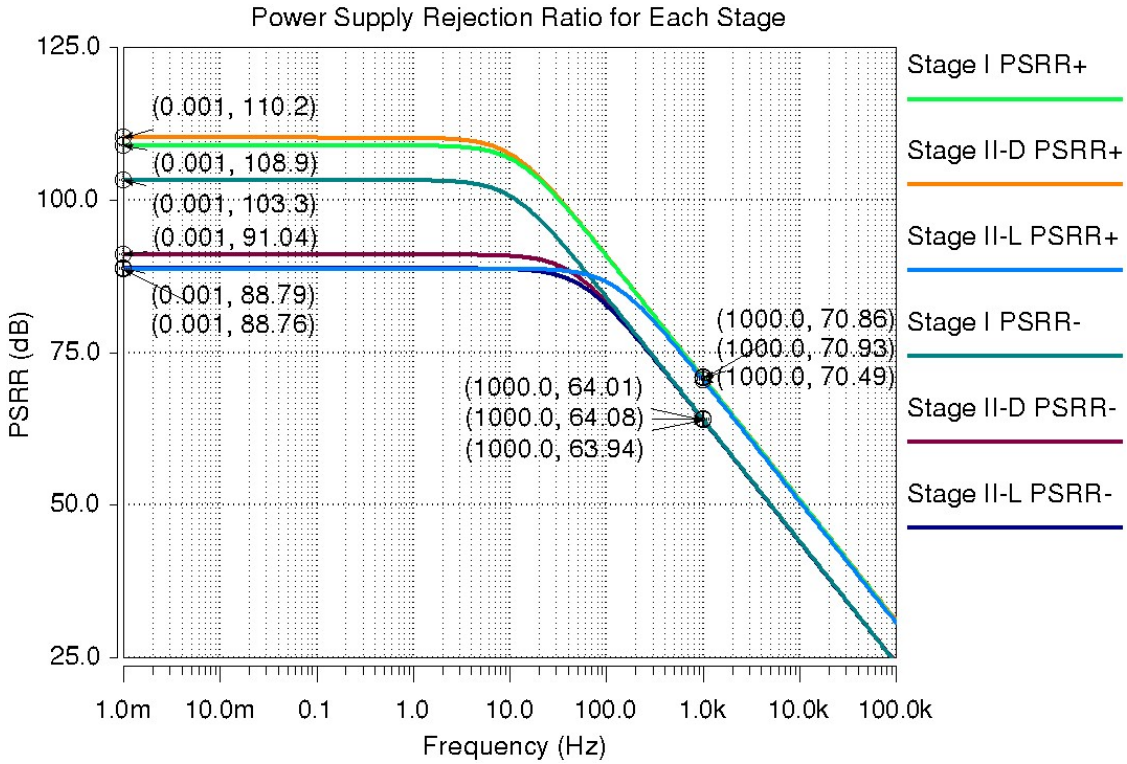



Fig. 4.14: Simulated power supply rejection ration (PSRR) for stage I and stage II using transistor design (D) and layout (L) values.

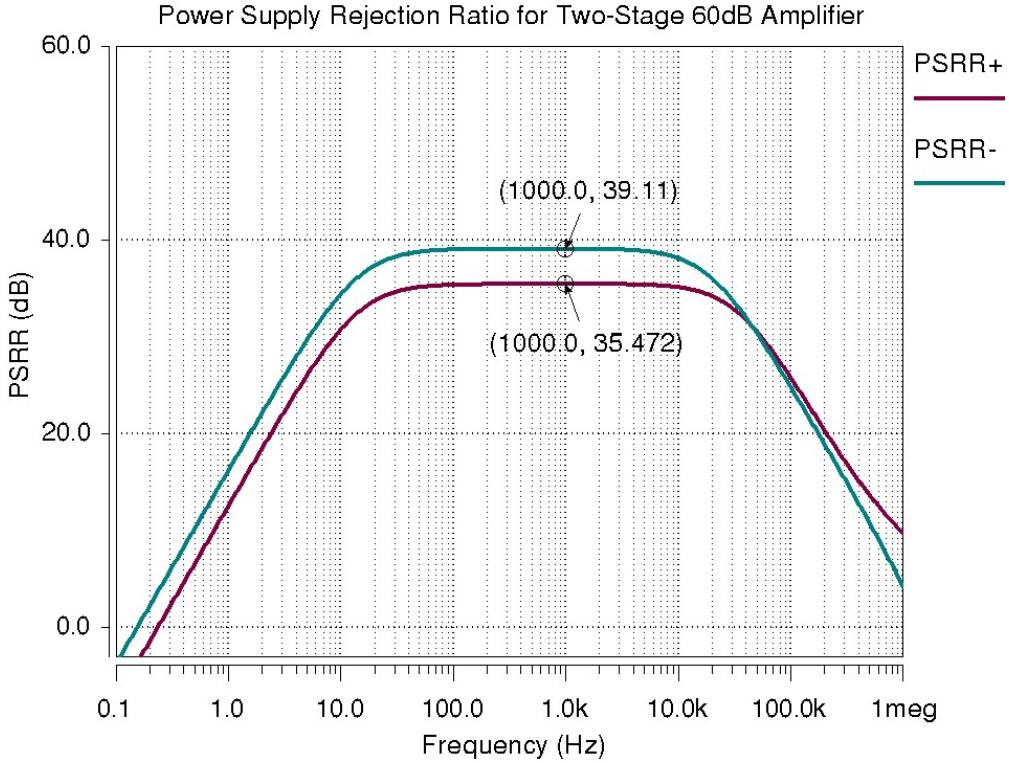



Fig. 4.15: Simulated power supply rejection ration (PSRR) for entire closed-loop amplifier using transistor layout values (see text).

#### 4.2.3.7 Offset Voltage

The simulated systematic output offset voltage of the closed-loop amplifier is expected to be near zero due to the open-loop design and feedback topology. This was verified for the typical model file and four process corners based on the simulated results printed in the operating point status of the output listing file as shown in Table 4.4. However, process variations in parameters of transistors matched in design will create offset voltages that are not accounted for by this simulation. Layout techniques of common-centroid configuration for the input transistors and symmetry for other matched devices were employed to reduce effects of random offsets.

**Table 4.4: Simulated Offset Voltage by Operating Point Status**

| Model File | Stage I Output Offset (µV) | Complete Amplifier Output Offset (µV) | Input Referred Offset Voltage (µV) |
|---|---|---|---|
| **Typical** | -0.004 | -19.352 | -0.019 |
| **Fast-Fast** | -0.194 | -15.981 | -0.016 |
| **Slow-Slow** | 0.067 | -20.705 | -0.021 |
| **Fast-Slow** | -1.378 | -27.794 | -0.028 |
| **Slow-Fast** | 0.063 | -16.447 | -0.016 |

Although the above simulation results as well as the simulations with pre-recorded neural signals show negligible offset, testing of the fabricated amplifier found unusual offset patterns. Additional simulations were performed to determine if the issue was present in the layout. Transient HSPICE simulations with sinusoidal inputs showed that the output exhibited, in addition to the expected amplification, an additional transient component which varied with parameters of the input signal (such as peak-to-peak voltage) and with the value set on the gate of MP2 (typically ground). This issue was also seen with each stage alone, so it was not due to the combination itself. Further investigations should be undertaken to understand the underlying causes of this issue.

#### 4.2.3.8 Dynamic Range

Graphs from simulation of dynamic range are presented in Fig. 4.16and Fig. 4.17. The input amplitude is over 1mV (2mVpp) before output clipping on the negative side.

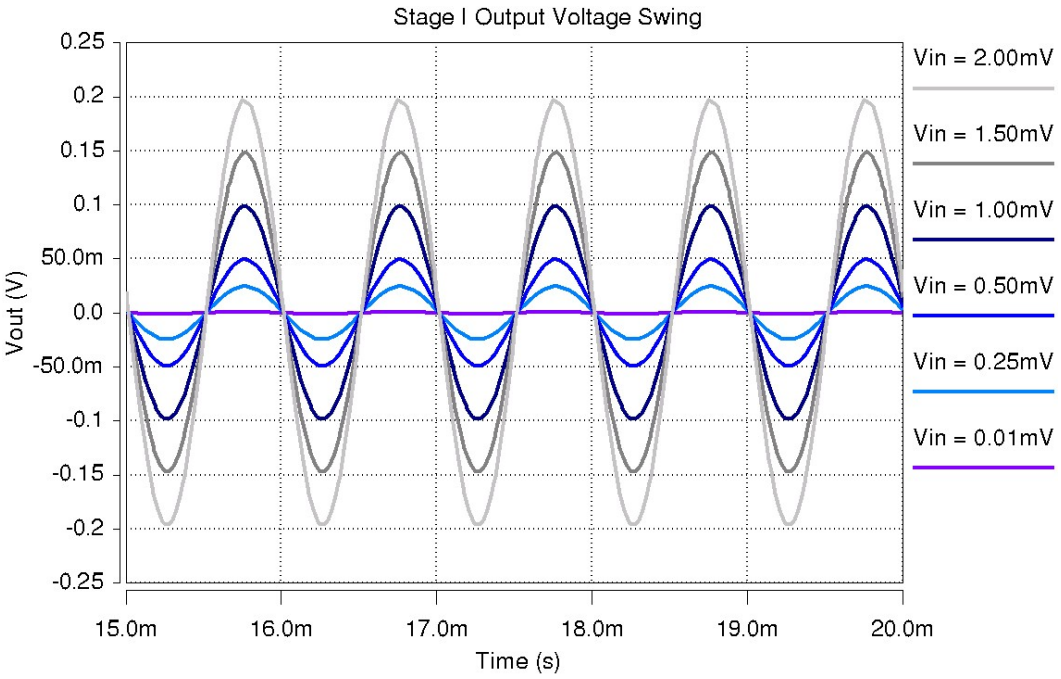



Fig. 4.16: Simulation for dynamic range of amplifier stage I. Vtune = 0V and Cload = 5pF. Input voltages are given in terms of amplitude; input frequency is 1kHz.

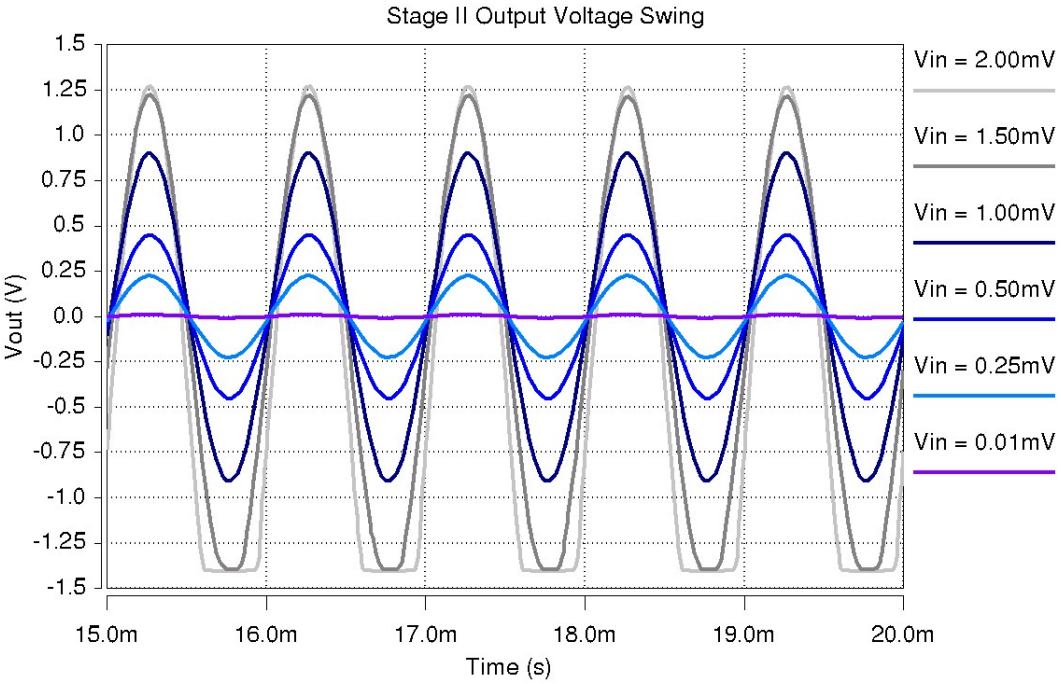



Fig. 4.17: Simulation for dynamic range of entire two-stage amplifier. Vtune = 0V and Cload = 5pF. Input voltages are given in terms of amplitude; input frequency is 1kHz.

#### 4.2.3.9 Simulated Response to Pre-Recorded Neural Signals

The amplifier was simulated with pre-recorded neural waveforms as diagramed in Fig. 4.18. The original pre-recorded signal (Vin1) was sampled at 20kHz. Since the amplifier also functions as a band-pass filter (BPF), the output (Vout1) should attenuate out-of-band signals. In order to observe how the amplifier responded (Vout2) solely to pre-recorded in-band signals, the input was ideally filtered (500Hz-5kHz) to create a second test signal (Vin2). Simulation results are shown in Fig. 4.19 and Fig. 4.20

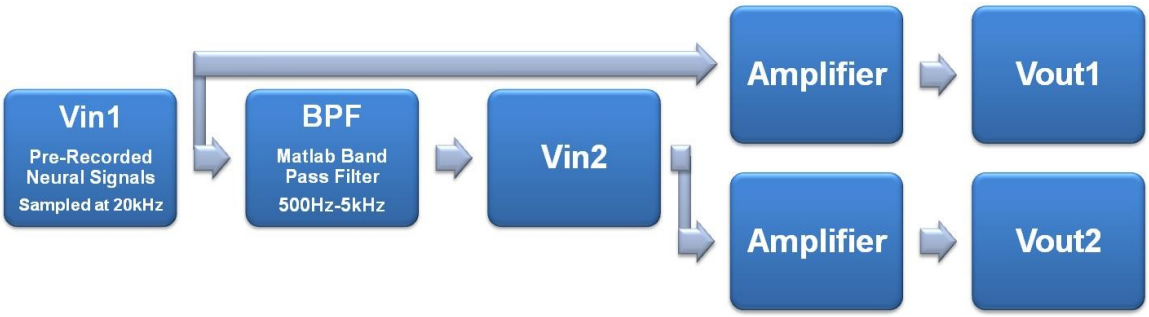



Fig. 4.18: Diagram showing correspondence between inputs and outputs for simulations with pre-recorded neural signals.

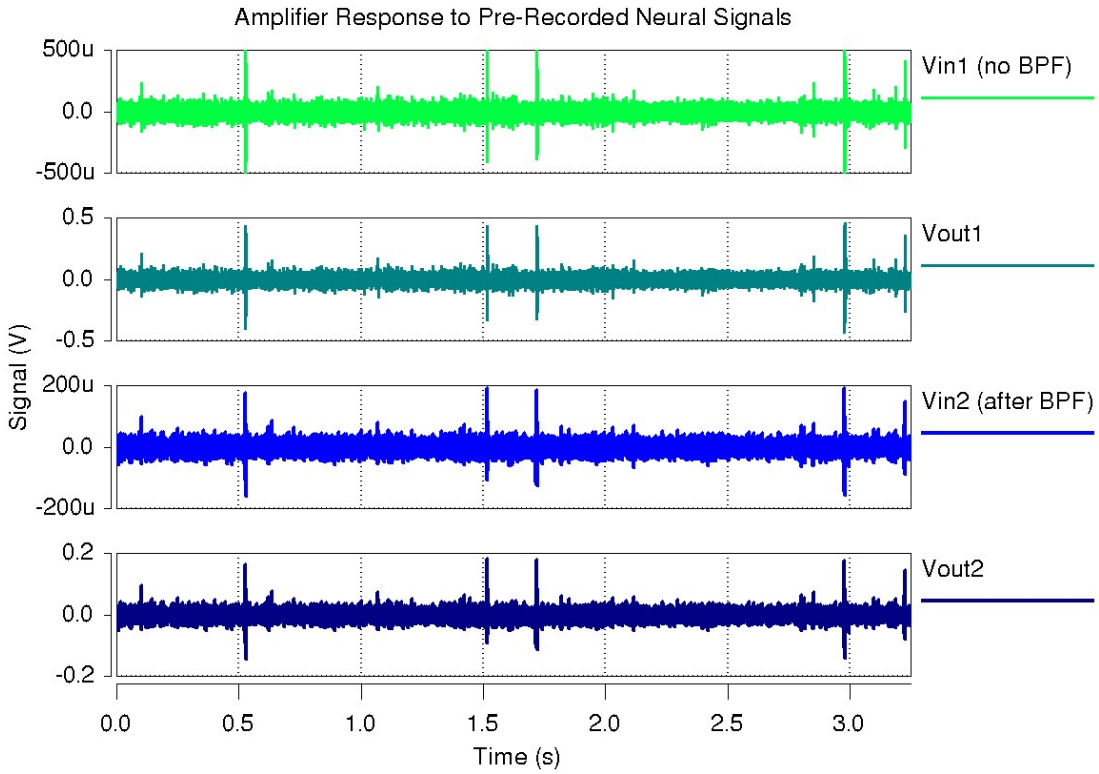



Fig. 4.19: Amplifier response to pre-recorded neural data with original (bright green) and band-pass filtered (bright blue) input signals.

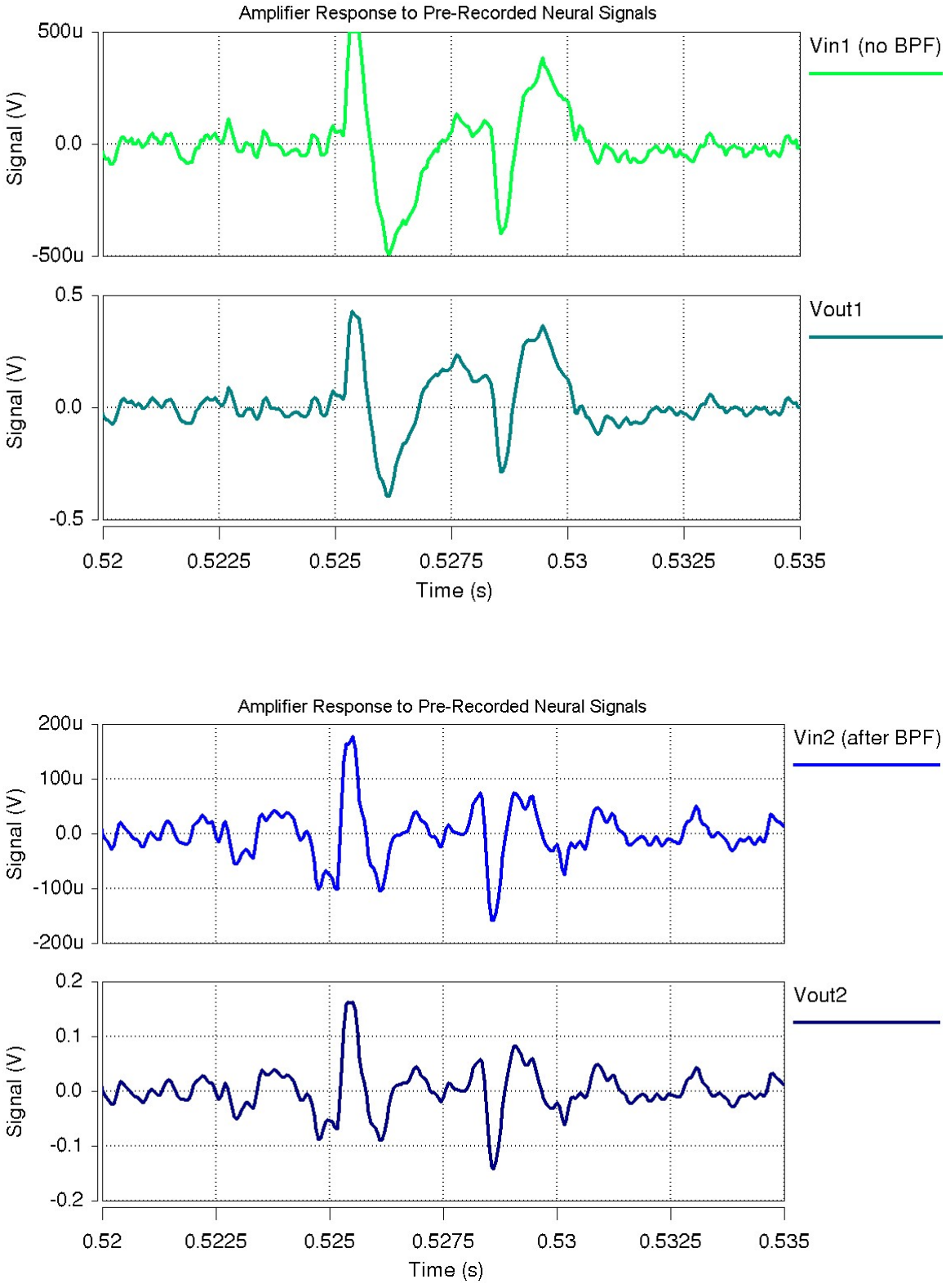



Fig. 4.20: Close-up of amplifier response to pre-recorded neural spike with original (bright green) and band-pass filtered (bright blue) input signals.

### 4.2.4 Measured Results for the Two-Stage 60dB Amplifier

A bank of 33 two-stage amplifiers, along with other circuitry, was fabricated in the AMI C5N CMOS process (0.5µm N-well, three-metal, two-poly) with the SCN3ME_SUBM option (now ON Semiconductor) through the MOSIS integrated circuit fabrication service. A photograph of the chip is presented in Fig. 4.22. The on-line wafer electrical test data and SPICE model parameters report NMOS and PMOS threshold voltages of 0.60V and -0.92V, respectively, placing the run near the modified fast-fast process corner (see Fig. 4.5). This section presents measured results from the fabricated chips.

#### 4.2.4.1 Power Dissipation

The fabricated amplifier bank (thirty-three amplifiers), the shared bias, and other circuits were supplied with current through the same power supply bond pads. The combined power consumption was measured for four chips with ground applied to the positive amplifier inputs and the feedback tuning node. The result for each chip was divided by thirty-three in order to determine the average power consumption of 46.53µW per amplifier. Since this measurement includes additional circuitry, the actual power dissipation per amplifier is less than the measured value. For a thirty-two channel system, this would correspond to less than 1.5mW. Fig. 4.21 compares the per-channel area and power of this design with two other reported neural recording amplifiers.

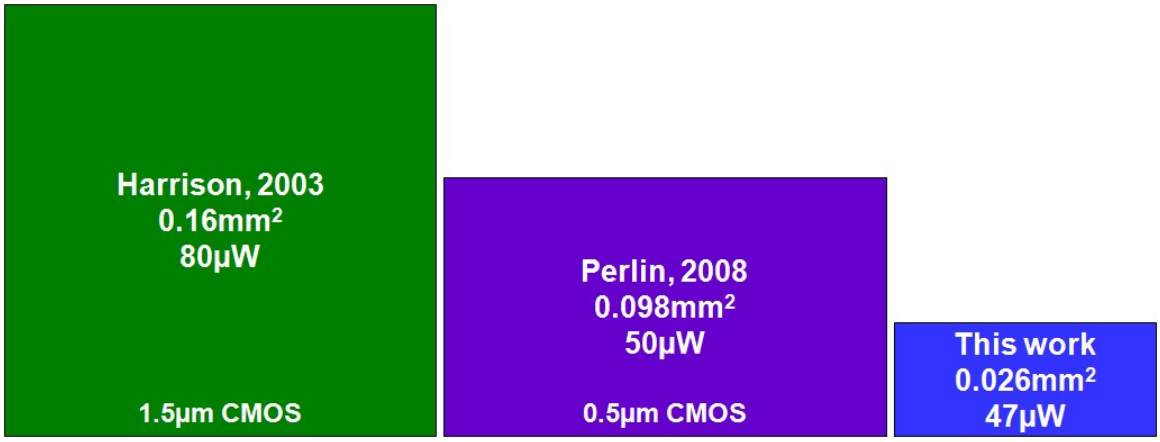



Fig. 4.21: Comparison of per channel size and measured power of neural recording amplifiers [59, 108].

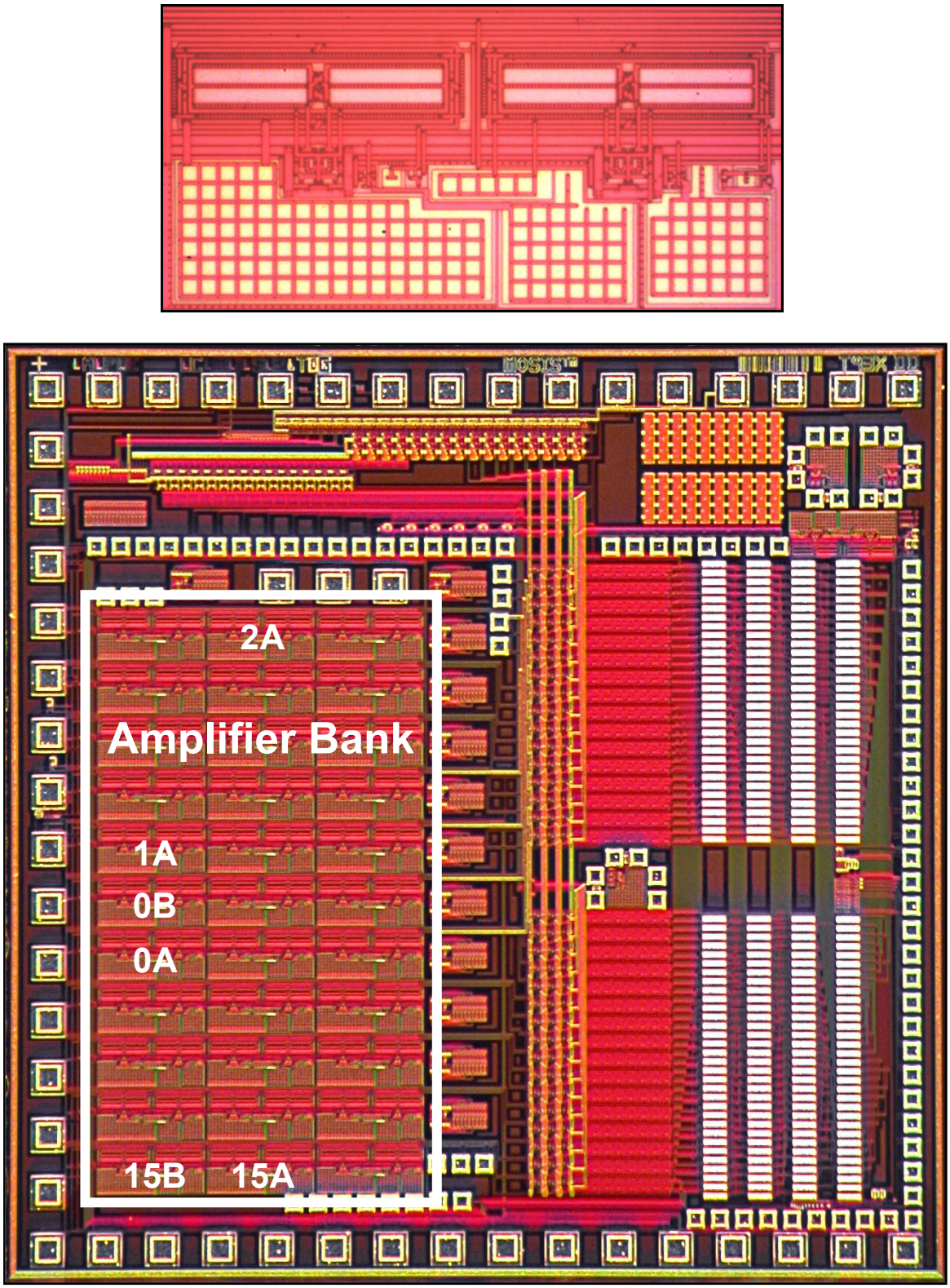



Fig. 4.22: Photographs of the fabricated two-stage 60dB neural recording amplifier (top) and full chip with bank of 33 amplifiers (bottom). Individual amplifiers used in measurement tests are labeled to show their location on the chip. The chip is 2mm by 2mm measured from the outside edge of the bond pads.

#### 4.2.4.2 Frequency Response & Low Cutoff Frequency Tuning

The HP4194A Impedance/Gain-Phase Analyzer was used to measure the amplifier frequency response; one *in vitro* gain spectrum is shown in Fig. 4.23. A LabVIEW program was written which interfaced with the 4194A through the GPIB (General Purpose Interface Bus) in order to record measurements.

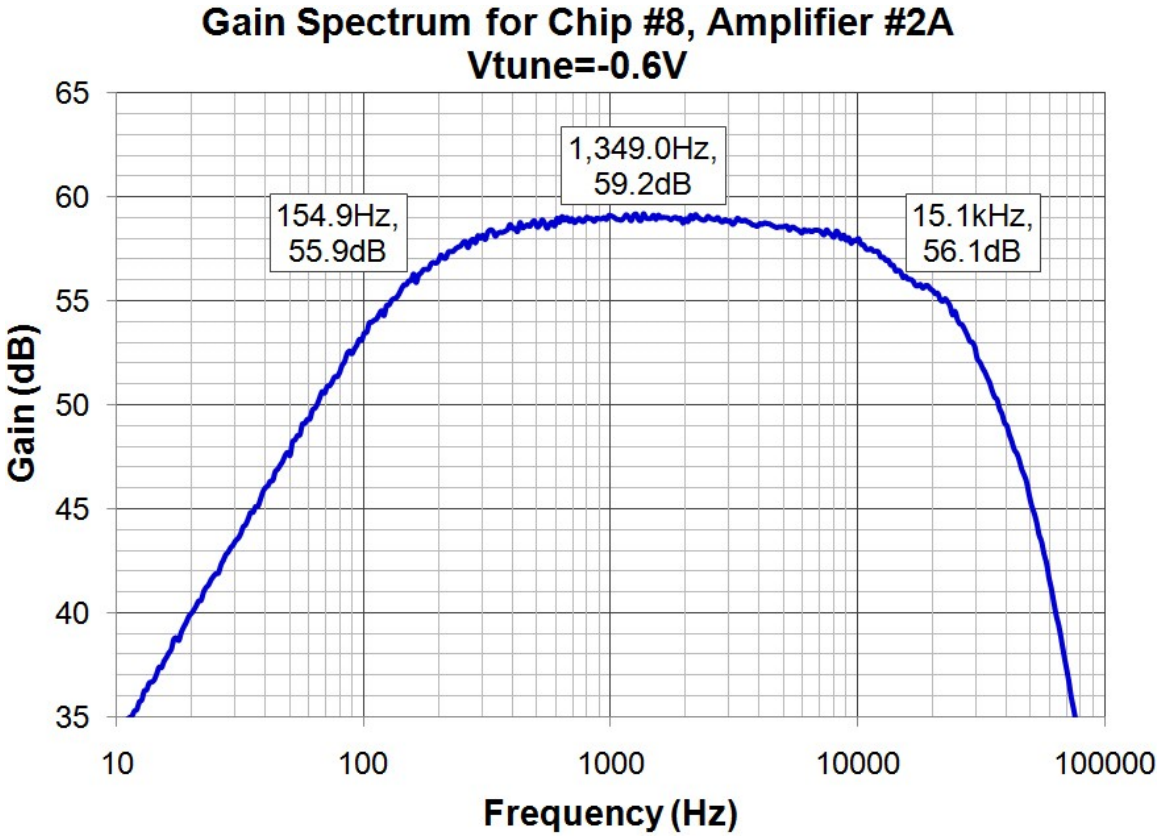



Fig. 4.23: Measured frequency response for chip #8, amplifier #2A with a tuning voltage of -0.6V applied to the gates of the feedback MOS-R to set the low cutoff frequency for recording neural action potentials.

The gain and high cutoff frequency was measured on six amplifiers across the amplifier bank on chip eight with the low cutoff tuning voltage set to -0.6V. The average measured in-band gain of 58.9dB was close to the simulated value. The gain was also repeatable with a sample standard deviation of 0.17. The mean high cutoff frequency was 21.3kHz. This was slightly higher than expected from simulations and can be reduced by increasing the compensation capacitors. The minimum possible low cutoff frequency (Vtune = 0V) is less than 10Hz and is thus below the frequency range of the HP4194A.

The amplifier was designed with an adjustable low cutoff frequency in order to make it suitable for recording local field potentials as well as neural spikes and to account for process variations in the resistance of the feedback transistors. Experimental data for the gain spectrum corresponding to a series of tuning voltages is displayed in Fig. 4.24. Although it merely conveys the input to output delay, the phase spectrum is also presented, since it demonstrates that there is no phase jitter. If desired, post-processing can be performed to remove any distortion due to the delay varying by frequency. An applied tuning voltage of -0.5V results in a cutoff frequency around 10Hz. As the magnitude of the tuning voltage is increased, the frequency of the low cutoff correspondingly increases. In order to amplify neural action potentials with this amplifier, a tuning voltage of -0.6V is ideal as this will reject both local field potentials and 60Hz noise. The low cutoff can also be raised above this for other applications.

The bandwidth tuning of six amplifiers spread across the amplifier bank on one chip were characterized and the measured results are shown in Fig. 4.25. The results also agree well with the simulated values, especially with a tuning voltage of -0.6 or less (magnitude) applied. It is presumed that part of the reason for this consistency is that the tuning voltage for the desired cutoff frequency is far enough away from the threshold voltages of the PMOS feedback transistors.

Another viewpoint on bandwidth tuning is to consider a particular frequency of interest and then observe how the tuning voltage modifies the amplifier gain at that frequency. In order to better visualize from this perspective, the 4194A was used to measure the gain during an externally triggered “sweep” of constant frequency. The applied tuning voltage was initially set to 0.1V and at each subsequent data point it was decreased by 0.01V. Fig. 4.26 displays the resulting graph for 10Hz, 100Hz, 1kHz, and 5kHz frequencies. As expected, at low magnitudes of tuning voltage the gain measures near the maximum in-band gain. Then at a “breakpoint voltage” associated with the frequency of interest, the gain begins to rolloff. As the tuning voltage becomes more negative, the gain (dB) decreases linearly with tuning voltage. At values of voltage past those plotted, the gain becomes less predictable since the voltage nears the threshold voltage of the MOS-R. However, these voltages are significantly beyond the range that would be used in a neural signal recording application.

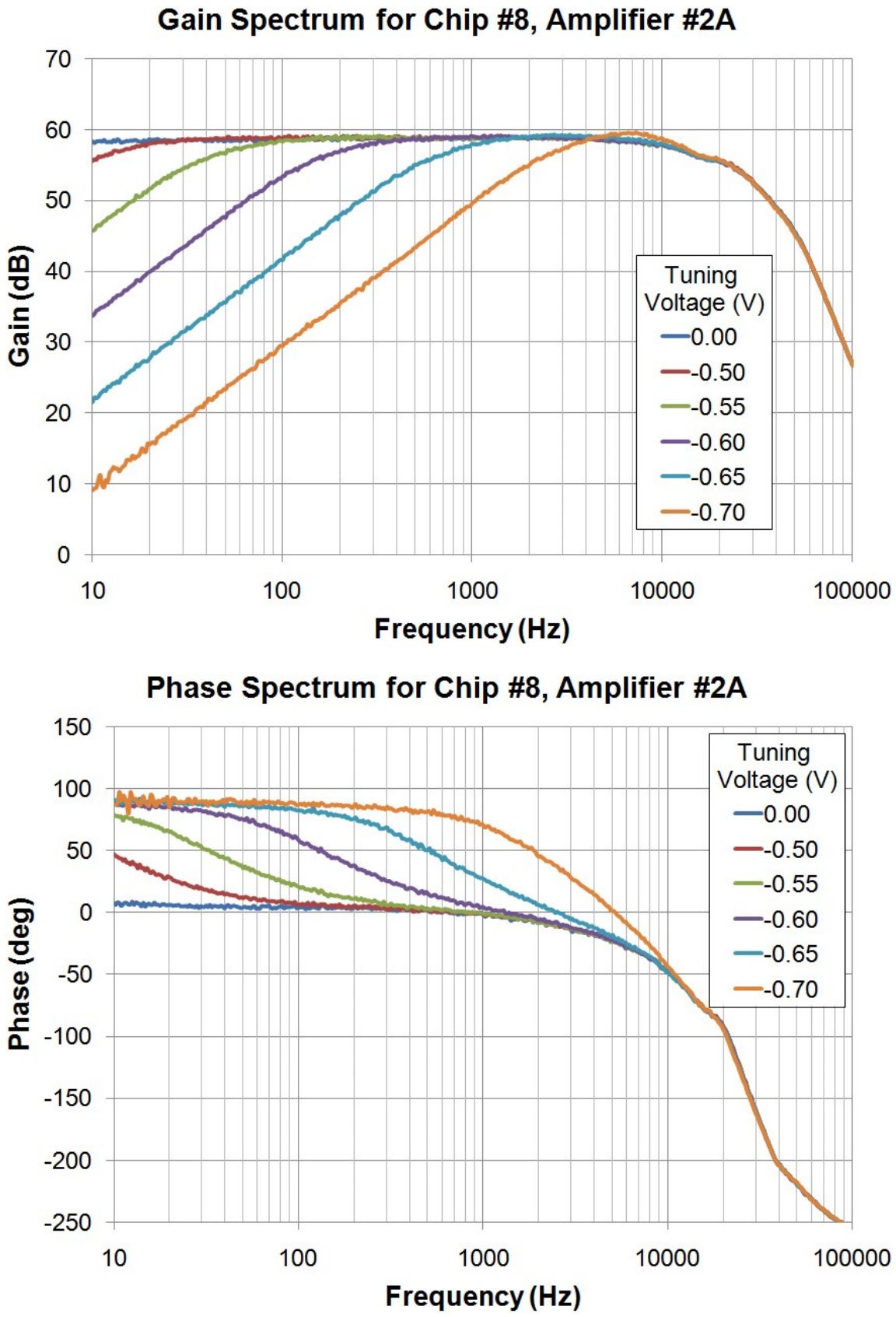



Fig. 4.24: Measured frequency response for chip #8, amplifier #2A.

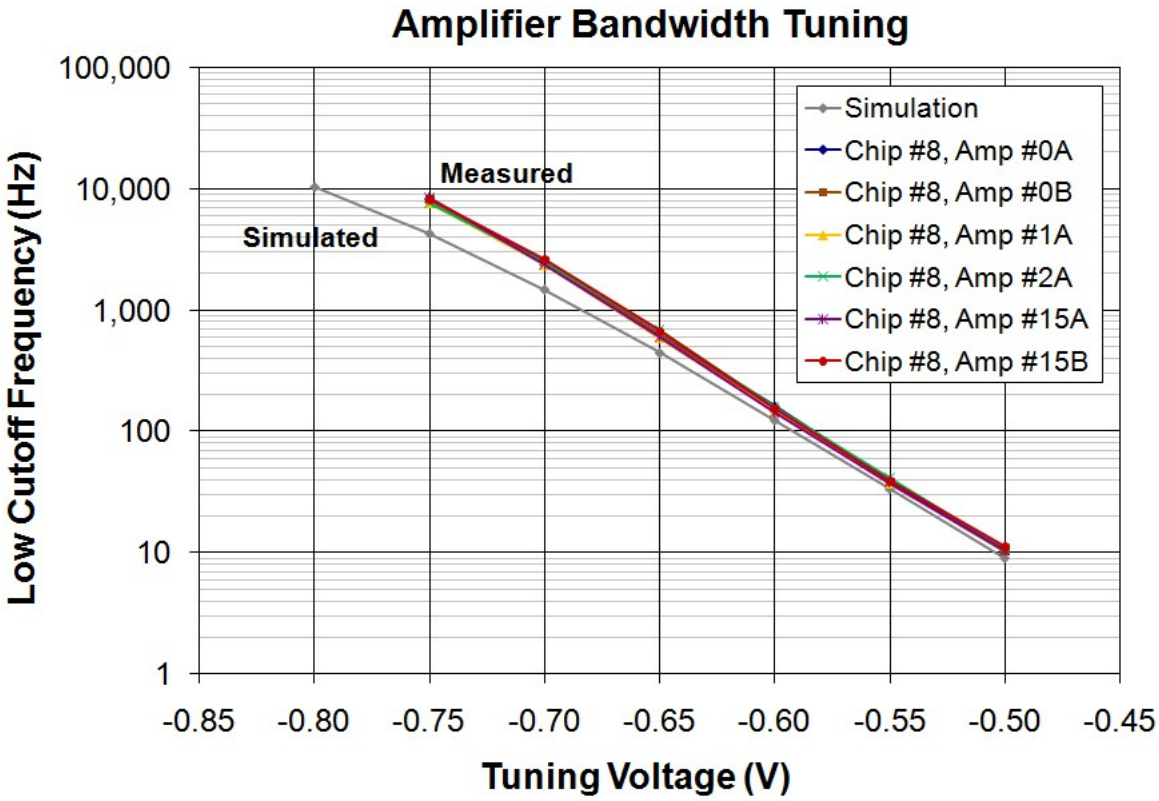



Fig. 4.25: Measured values of low cutoff frequency as a function of tuning voltage from six amplifiers on chip #8 in comparison to simulated values.

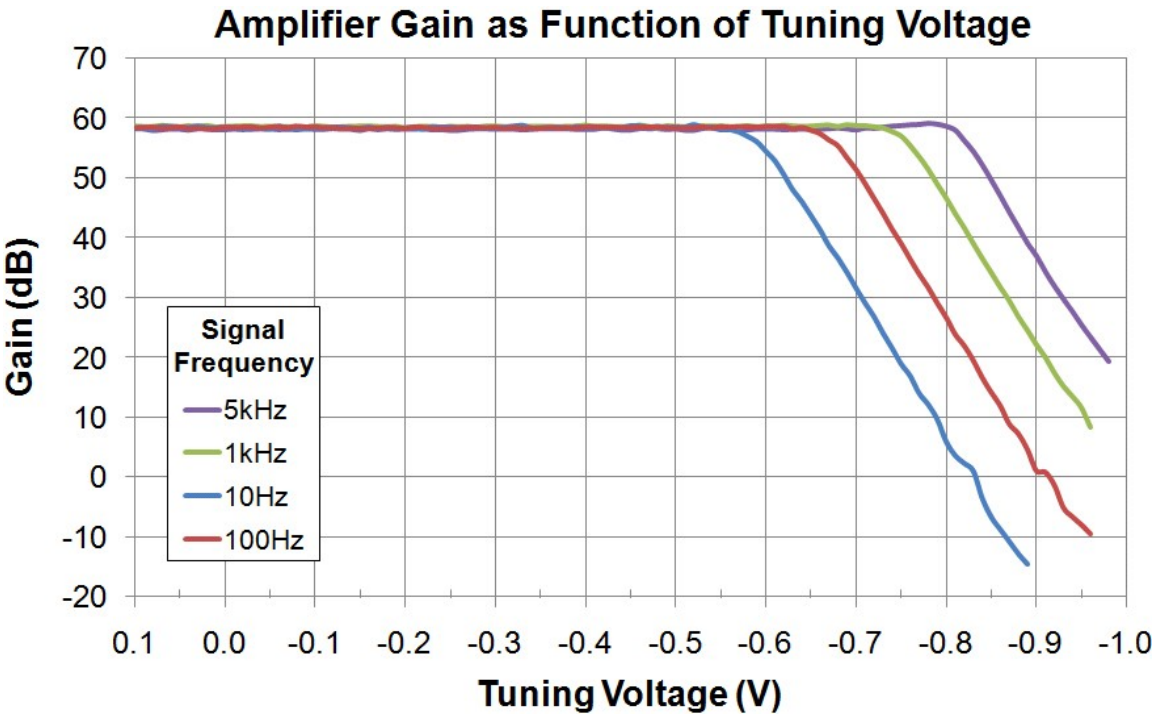



Fig. 4.26: Measured values of gain (chip #8, amplifier #0A) at four frequencies with a sweep of the low cutoff tuning voltage from 0.1V downward in -0.01V steps.

#### 4.2.4.3 Power Supply Voltage and Rejection Ratio

The ability to function with variations in supply voltage is necessary for circuits powered by telemetry or battery. The 0.5µm technology used for this chip is intended for a maximum supply voltage of 5V. Two types of tests were used to investigate the *in vitro* characteristics of this amplifier in regards to supply voltage: DC supply value and AC supply ripple.

The first experiment changed the rail-to-rail voltage (Vdd-Vss) from 2V to 4V. The ground supplied to the chip was halfway between the rails. The 4194A was used to measure the gain for each data point. Fig. 4.27 graphically shows the result. The gain is relatively stable for a decrease in supply voltage up to 20% and for an increase in supply voltage up to 10%.

The second investigation was the power supply rejection ratio (PSRR). With the input grounded, a small AC signal (2mVpp) was placed on one of the supply lines and the supply gain (Vout/Vsupply) was measured with the 4194A from 100Hz to 20kHz in 100Hz steps as shown in Fig. 4.28; both the frequency of the supply ripple and the measurement frequency were changed simultaneously. Then the same procedure was used to measure the gain (Vout/Vin) of the amplifier. Two or three trials of each were taken and averaged. The PSRR was calculated as $(V_{out}/V_{supply})^{-1}/(\text{Gain Spectrum})^{-1}$ and is graphed in Fig. 4.29. The positive and negative PSRR at 1kHz are 59.6dB and 41.9dB respectively.

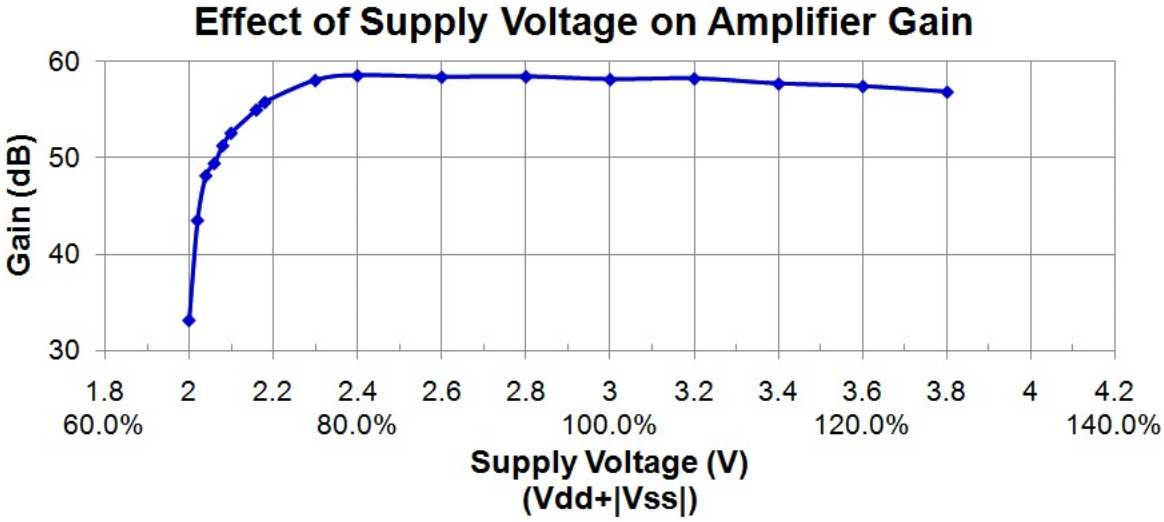



Fig. 4.27: Measured values of amplifier gain as the power supply voltage is changed.

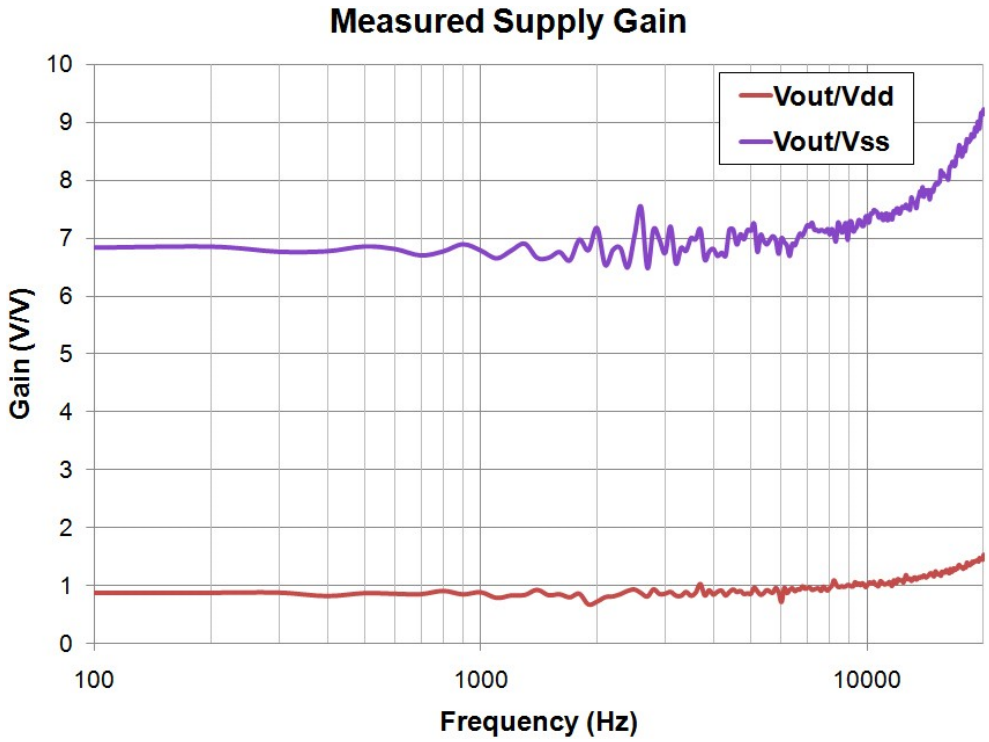



Fig. 4.28: Measured frequency response with 2mVpp AC variation on the supply lines.

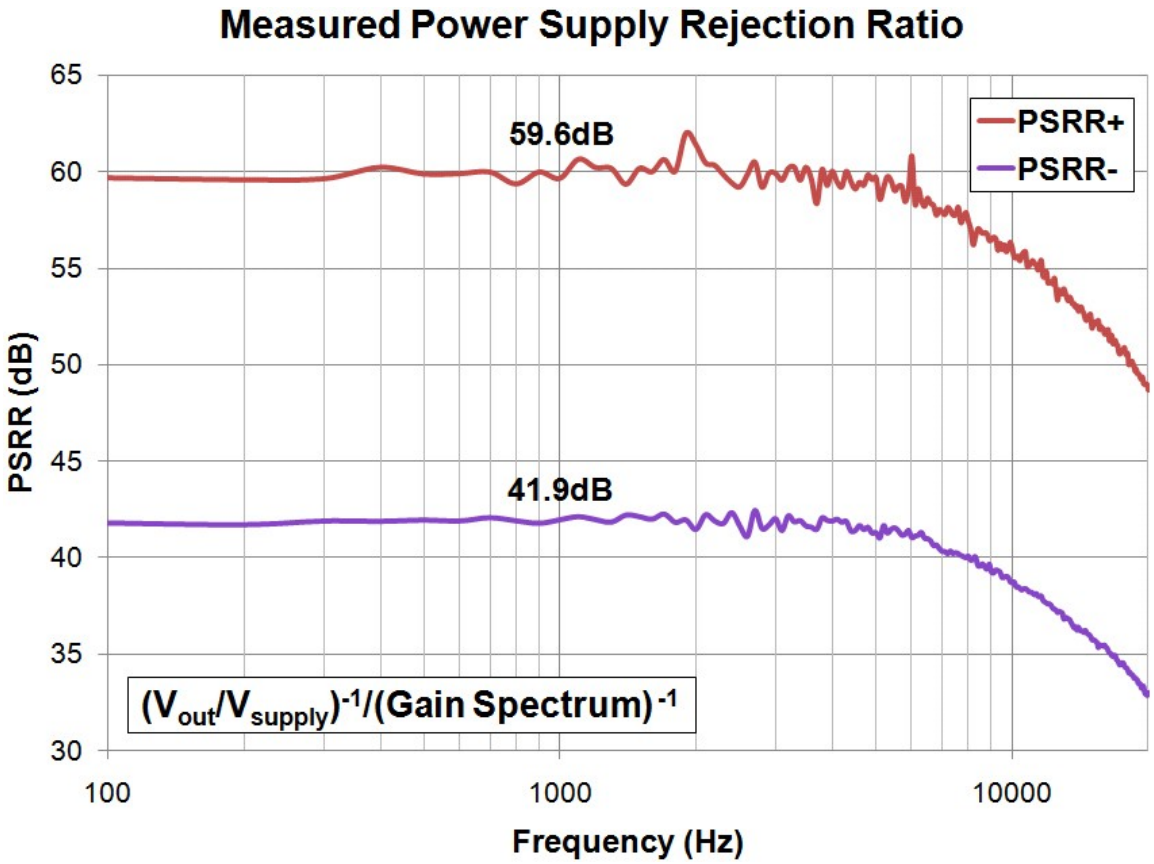



Fig. 4.29: Measured power supply rejection ratio; the values at 1kHz are labeled.

#### 4.2.4.4 DC Rejection

An amplifier topology which rejects the DC component of the signal at the electrode site is essential since this value can be ±50mV and vary not only from site to site but also over time [57, 105]. Various approaches have been taken to meet this requirement. The AC coupling used in this amplifier was chosen since the input capacitor provides a simple means to perform this function and set the gain. This methodology also enables a low cutoff frequency to still be achieved when desired by setting the tuning voltage of the feedback transistors. To validate that the amplifier rejects DC components, 1kHz signals with ~2mVpp inputs and varied DC offsets, up to ±1Vdc were applied at the input and the outputs were recorded. Fig. 4.30 shows both the inputs and resulting amplified signals. As expected the input offsets are rejected.

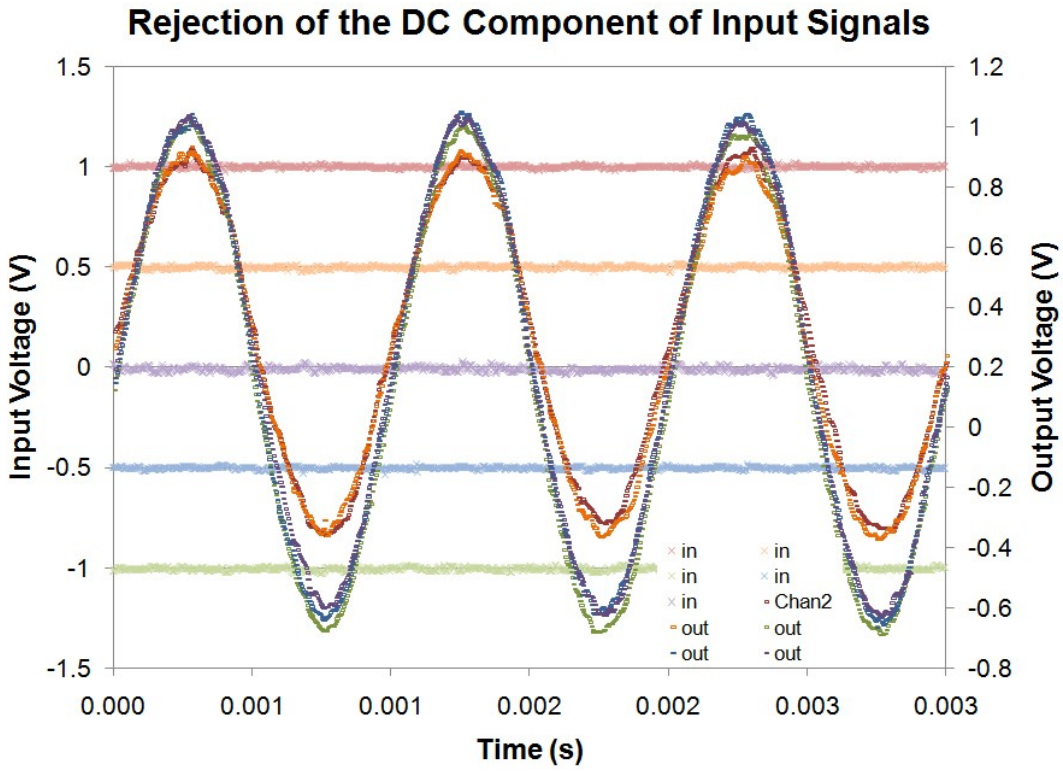



Fig. 4.30: Measured response to ~2mVpp input signals at 1kHz with DC offsets. The pastel colors are the input signals and the corresponding bold colors are the respective outputs.

#### 4.2.4.5 Dynamic Range

Output signal distortion and clipping both limit the useful range of input signals. One major contribution to this situation is the range of the supply voltage that was chosen since the output can not exceed the supply rails and the transistors between the output node and supply lines need a minimum voltage drop. Schematic design selects the transistor placements and biasing and thus the dynamic range. The other major contributor is amplifier gain. With a gain of 1000 and a 3V supply (±1.5V), even if no headroom was necessary, the maximum theoretical input signal that would be ideally amplified would be 3mVpp. Signals at 1kHz with a peak-to-peak voltage up to 3.5mV were used as inputs and the outputs were recorded as graphed in Fig. 4.31. Outputs corresponding to inputs above 2.5mVpp exhibit distortion on the negative portion of the wave and clipping on the positive side. With a 2.5mVpp input, the output swings from 1.46V to -0.95V.

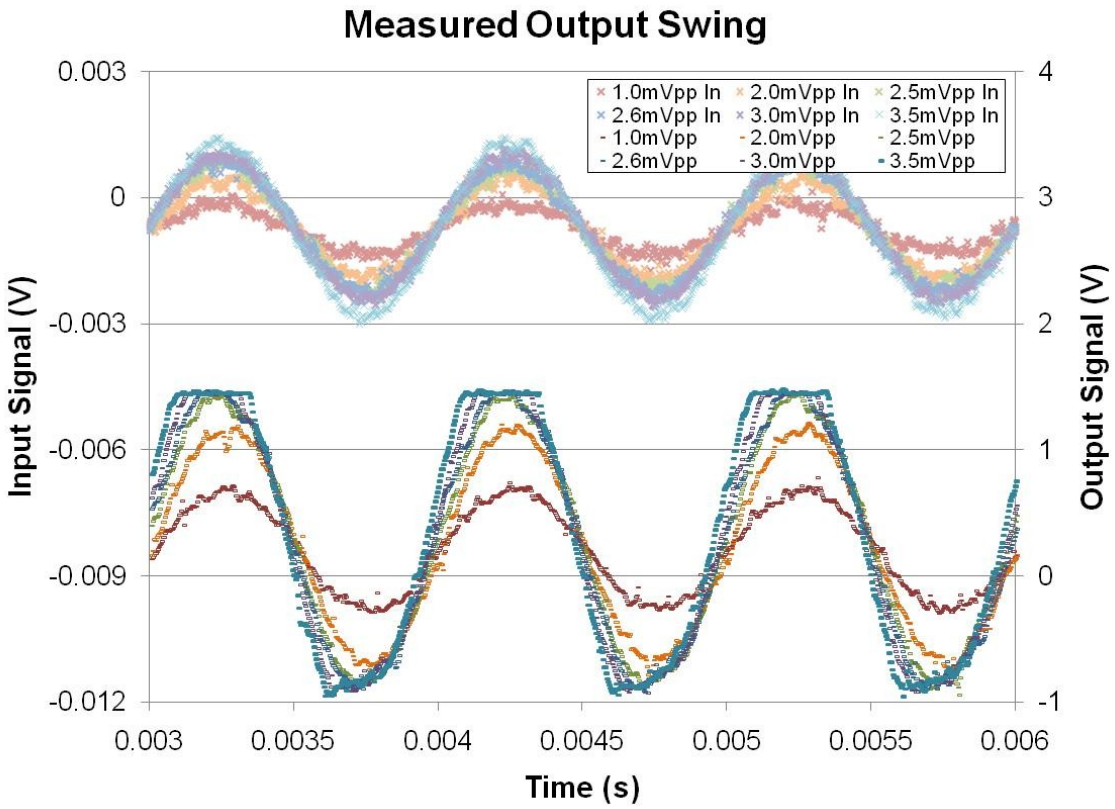



Fig. 4.31: Measured output swing. The pastel colors are the input signals and the corresponding bold colors are the respective outputs.

#### 4.2.4.6 Measured Response to Pre-Recorded Neural Signals

In spite the effectiveness of sinusoidal input signals for understanding the operation of a circuit, the final verification of proper performance is within the application for which it was designed. Pre-recorded neural signals were therefore used to confirm that the amplifier does indeed function for neural recording. The pre-recorded signal was the same one used in simulations above. A 0.8s segment of the data was uploaded into the waveform generator which was connected to the input node and oscilloscope. Fig. 4.32 shows the waveform generator data and the output data captured from the oscilloscope (see Fig. 4.19). Fig. 4.33 and Fig. 4.34 (see Fig. 4.20) present close-ups of the neural spike. Although there is an offset present on the output, the waveform shape is in remarkable conformity to the scaled input and with no noticeable delay.

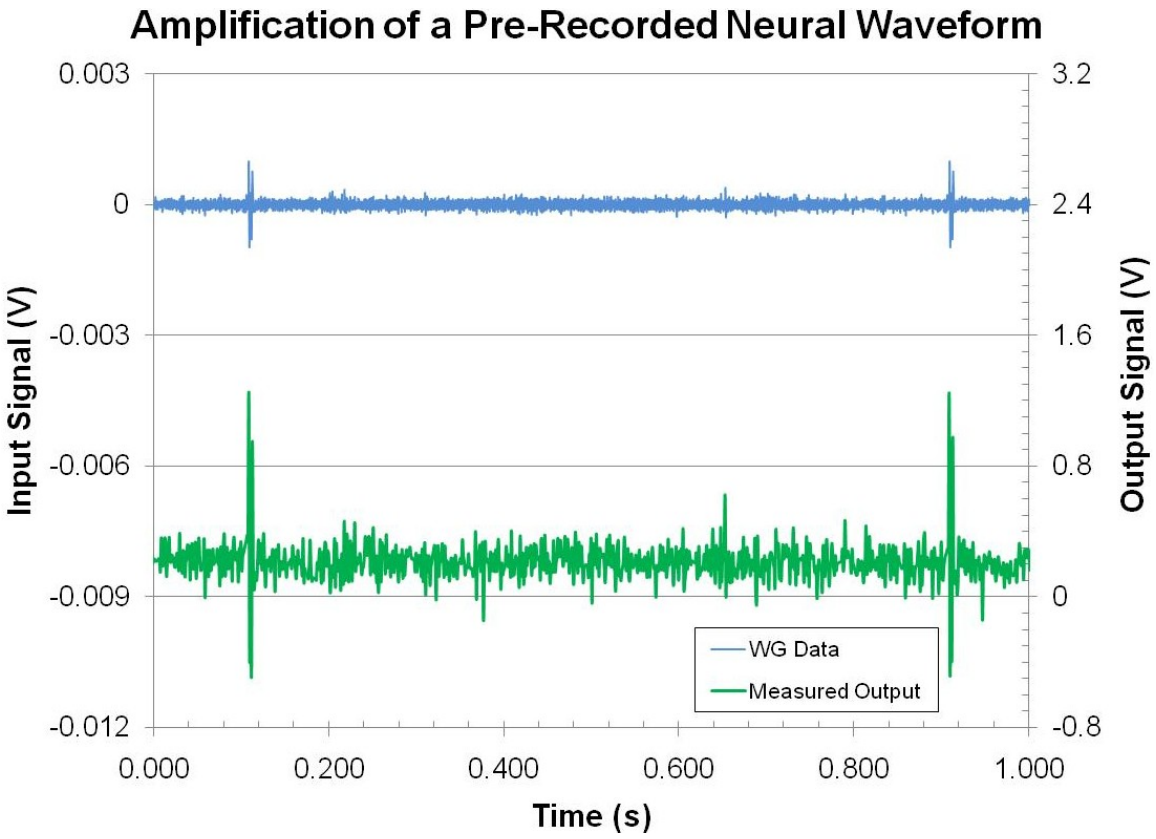



Fig. 4.32: Measurement with a pre-recorded neural signal. The waveform generator (WG) data (blue, top) was twice the amplitude of the original 0.8sec pre-recorded data which was sampled at 20kHz. The measured output (green) shows that circuit is able to detect and amplify the neural spike.

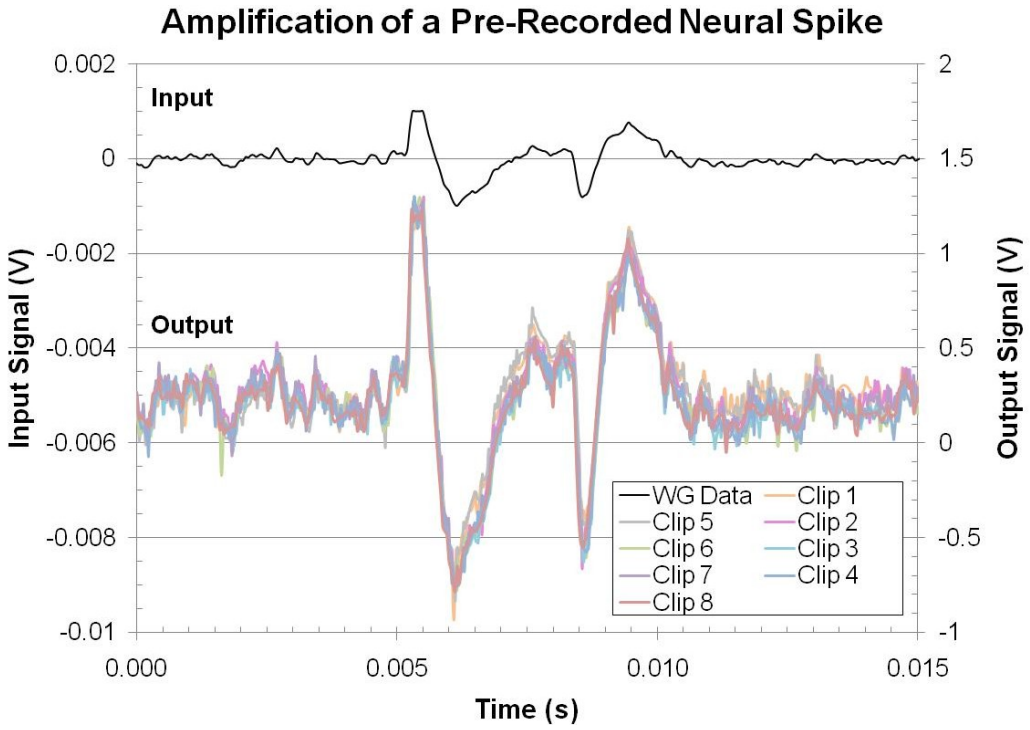



Fig. 4.33: *In vitro* amplification (captured eight times) of a pre-recorded neural spike. The waveform generator data (black) was twice the amplitude of the original data.

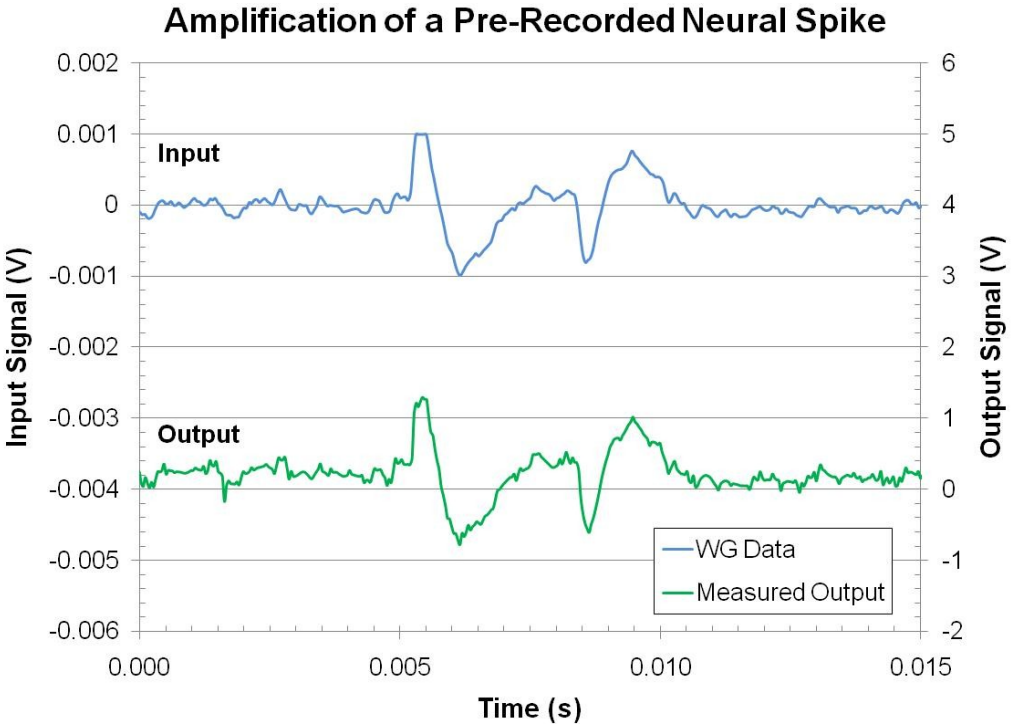



Fig. 4.34: Measured *in vitro* amplification (green) of a single pre-recorded neural action potential. The waveform generator (WG) data (blue) was twice the amplitude of the original data.

### 4.2.5 Amplifier Parameter Summary

A new low-power low-area neural recording amplifier has been designed and tested *in vitro* with test signals and pre-recorded neural waveforms. Table 4.5 provides a summary of the simulated and measured amplifier parameters. The measured values indicated that the fabricated performance metrics are near the expected values based on simulations. One issues, the output offset voltage remains to be fully understood. Further simulations and testing should be done to determine the cause. The main disadvantage of an output offset is felt when switching from one channel to another in a multiplexed situation since it can cause saturation. Further characterization should also be done to determine the amplifier noise level and for *in vivo* testing. If this amplifier was used in a thirty-two channel system the total static power consumed by the recoding bank would be less than 1.5mW and the area would be less than 0.9mm$^2$.

**Table 4.5: Summary of Amplifier Characteristics**

| Parameter | Simulated | Measured |
|---|---|---|
| **Process** | 0.5µm CMOS | |
| **Die Area per Amplifier** | 0.0255mm$^2$ | |
| **Supply Voltage** | ±1.5V, ground | |
| **Power Consumption** | 51.51µW | < 46.53µW |
| **Open-Loop Gain** | 99.3dB stage I<br>82.6dB stage II | --- |
| **Closed-Loop In-Band Gain** | 59.2dB | 58.9dB<br>(N = 6, σ = 0.17) |
| **DC Rejection Range** | --- | >±1V |
| **Lowest Low Cutoff Frequency** | 3.5µHz | <10Hz |
| **Low Cutoff Frequency Tunability** | Yes | Yes<br>< 10Hz to > 5kHz |
| **High Cutoff Frequency** | 9.9kHz<br>(Vtune = -0.6V) | 21.3kHz<br>(Vtune = -0.6V) |
| **Output Voltage Swing** | 1.46V to -1.33V | 1.46V to -0.95V (before visible distortion) |
| **Power Supply Rejection Ratio at 1kHz** | 35.5dB (PSRR+)<br>39.1dB (PSRR-) | 59.6dB (PSRR+)<br>41.9dB (PSRR-) |

# CHAPTER V

# A THREE-DIMENSIONAL FOLDING ASSEMBLY STRUCTURE UTILIZING PLANAR FABRICATION

Penetrating probes and structural MEMS components are key elements of electrode arrays. Planar fabrication technology is currently used to batch-fabricate multi-shank probes with electrodes arrayed in two dimensions. Techniques to form three-dimensional arrays from such two-dimensional probes typically require inserting individual 2-D probes into separate platforms. This chapter describes an alternative method in which probes and platforms are integrated as a single unit resulting in a low-profile and narrow-platform design. The fabrication was done at the University of Michigan Lurie Nanofabrication Facility (LNF) by Dr. Onnop Srivannavit and Mrs. Mayurachat (Ning) Gulari. Scanning electron microscope (SEM) images of these arrays were taken at the University of Michigan North Campus Electron Microbeam Analysis Laboratory (EMAL) with the assistance of O. Srivannavit and N. Gulari.

## 5.1 Folding Structures

Creating three-dimensional structures out of two-dimensional sheets is at least as old as origami. Over the years, the application of this technique to diverse fields has yielded some original architectures and devices. One example in the field of MEMS is the use of "pop-up" assembly with constraining hinges to form raised structures such as the one illustrated in Fig. 5.1 [112].

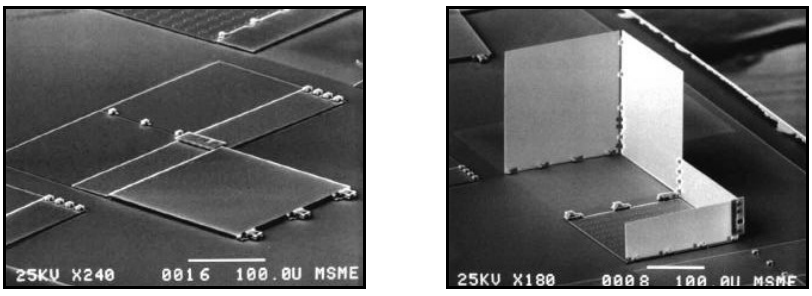



Fig. 5.1: A pop-up corner-cube-reflector, planar (left) and assembled (right) [112].

As a preface to future possibilities, the folding concept was employed by Rouche, et. al., in a six-shank, twelve-site electrode array shown in Fig. 5.2 [113]. In this design, the interconnect leads do not cross the fold so there is a separate cable leaving the array for each "probe." As such, the cables must be twisted ninety degrees in order to lay flat on the surface of the brain. Since the substrate of the whole device is polyimide, before implantation, incisions in the *pia* must be made which match the shank positions to prevent shank buckling during insertion. While this may be feasible for a low shank count, it becomes less practical as the array density increases.

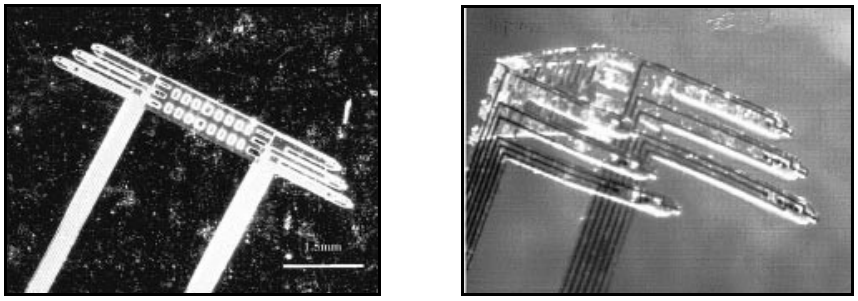


Fig. 5.2: Six-shank polyimide array, flat (left) and bent into 3-D shape (right) [113].

Researchers at the University of Tokyo developed a polyimide folding array [114]. An electroplated nickel layer (5µm thick) was included on the back-side of the shanks to enable batch folding by applying an external magnetic field. The nickel-backing also increased the device stiffness for ease of insertion. However, the exposed nickel could cause biocompatibility issues for chronic *in vivo* use. The shank lengths and "probe-to-probe" spacing constrain each other with the 2-D layout presented in Fig. 5.3.

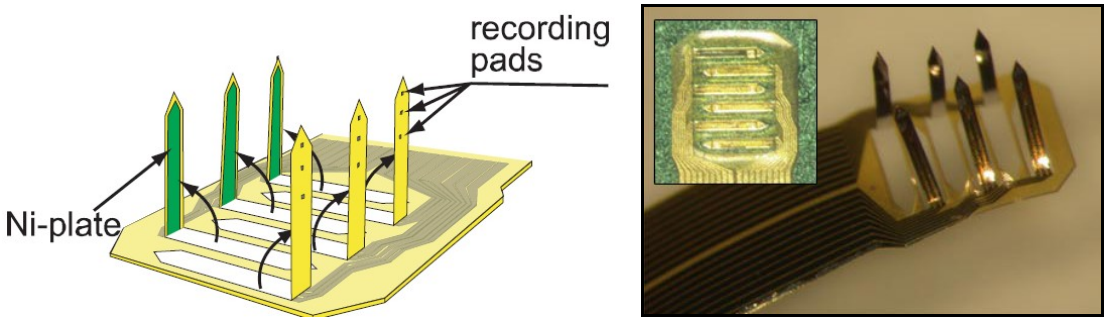



Fig. 5.3: Conceptual sketch (left) of a 3-D array achieved by folding the probe shanks using a magnetic field [114]. Photographs of the device before (inset) and after (right) assembly.

The idea of foldable interconnects was exploited by Yao, et. al., to create a low-profile electrode array with integrated CMOS circuits on the probe back-ends [115]. This design utilizes gold beams encapsulated in a parylene sheath to form the bendable area. Multiple silicon braces mark positions for bending which enables stacked final heights. A custom jig is used to fold the probes before insertion into the platform. Spacers with snaps and key latches secure the back-end at the designated height. This work reports a wafer-level process including parylene encapsulation prior to the boron etch-stop release.

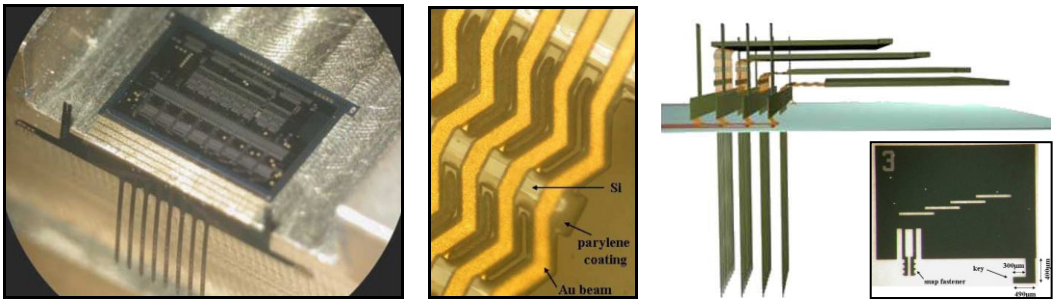



Fig. 5.4: Probe with folding back-end (left) due to encapsulated gold beams and silicon braces (middle) used with spacers to create a low-profile array (right) [115].

The folding concept was also used by researchers at National Tsing Hua University to develop a 3-D array made of SU8 (mechanical stiffness) and Parylene (encapsulation and hinges) [116]. To decrease insertion challenges, array joints were fixed in polyethylene glycol (PEG), which dissolves after implantation, by injecting it through the microchannel. These devices were assembled by an electrostatic actuation, using a field up to 8kV. The photographs of the folded devices, presented in Fig. 5.5, show shank curvature and a large-area platform which could cause *in vivo* challenges.

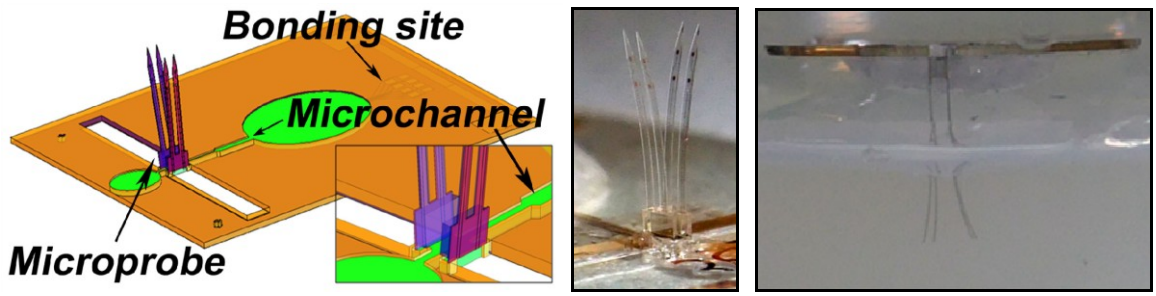



Fig. 5.5: Conceptual sketch (left) of a 3-D array achieved by folding the probes using a electrostatic actuation [116]. Photographs of the folded device (center) and implanted in bio-gel showing its broad platform (right).

## 5.2 Conceptual Overview of the Folding Assembly Structure

The MEMS Folding Assembly Structure (FAST) is a design-for-assembly layout approach which enables the formation of small, three-dimensional devices with electrical interconnections. The FAST scheme can be applied to electrode arrays to integrate individual probes, electrical interconnects, and their corresponding platforms directly at the device layout level. This structural development decreases lateral platform size and vertical rise. Reduced assembly time and increased yield are also target objectives of the technique.

Whereas previous three-dimensional designs require inserting individual two-dimensional probes into a mounting platform, the FAST technique allows already connected probes and platforms to be folded into position. For example, a FAST electrode array could combine what traditionally would be thought of as four, two-dimensional probes and the portion of the mounting platforms that would span the space between them, as illustrated in Fig. 5.6.

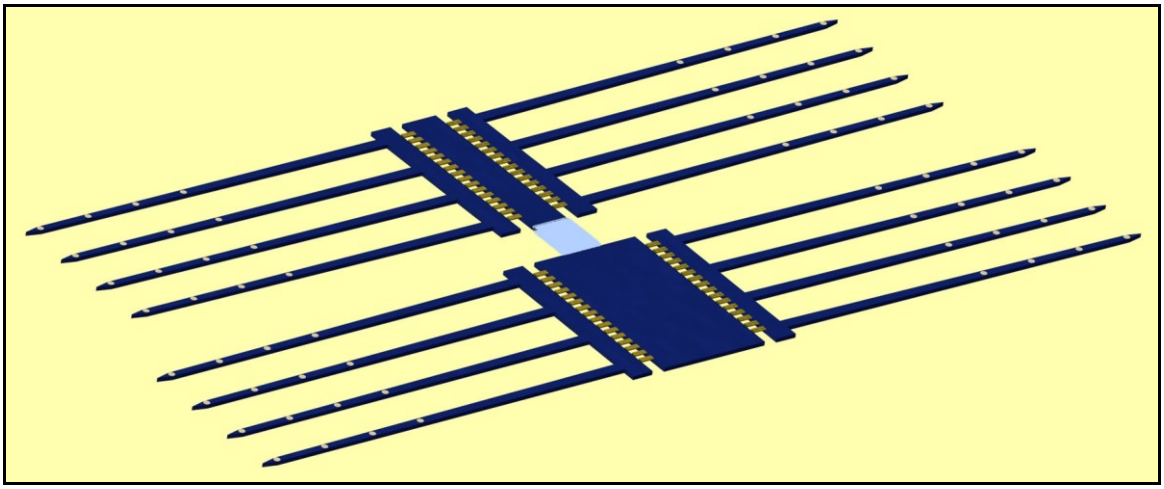


Fig. 5.6: Example of one planar Folding Assembly Structure (FAST) layout design.

The interconnect leads are routed from the individual electrode sites to the probe back-end and then across foldable interconnect to the associated platform, eliminating the first stage of interconnect bonds which the structure by Perlin requires [59]. When four probes are incorporated into one array, the leads from the smaller, bottom platform can travel across the foldable platform connector cable to the wider, top platform, and then all of the leads can come off the array on a single cable. Alternately, individual flexible

cables can leave the array from both the top and bottom platforms. Since the cables exit the array parallel to the platform, they may lay flat on the surface of the brain. These flexible cables are used to bring leads from the array platform stack to a remote location. Remaining lead transfers follow a process similar to previous designs.

The corresponding assembly process is illustrated in Fig. 5.7. Assembly begins with the fabricated planar array. The two-probe units are folded onto each other, stacking the smaller, bottom platform vertically on top of the larger, top platform. Since the individual platforms are thin (approximately 25µm including the interconnect and insulating layers), this stacking does not significantly increase the overall height. Then the four probes are bent orthogonal to the platform and secured. The overall vertical rise is a combination of the height due to the probe back-end, foldable interconnects, and platform. The lateral dimension of the platform is virtually confined to the area of tissue instrumented; no platform overhang is necessary as in a slot assembly method. The order of the folds is variable; since foldable structures other than the four-probe example given are possible, the best assembly procedure depends upon the overall design.

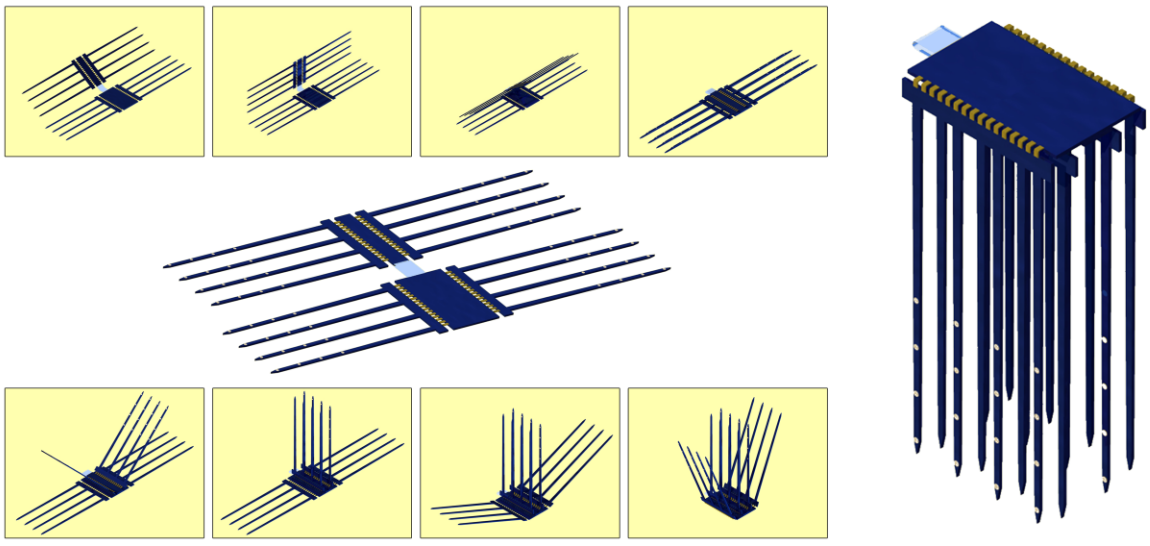


Fig. 5.7: Conceptual process of the FAST assembly using the example layout.

Placing circuitry close to an array is often desirable. If an active fabrication process is used, circuits may be incorporated directly on the probe back-end, the platform, an extension to the platform, or in another location reached by integrated or hybrid cables. Similarly, hybrid chips may be incorporated on the platform, an extension

to the platform, or at a location reached by cables. Connections to the hybrid chips may be achieved by methods such as wire bonding or beam-lead interconnects.

The number of electrode sites and shanks as well as dimensions may be varied as application requires, although minimum platform width becomes constrained by lead line number and pitch. Multiplexing circuitry located on the array would be advantageous to decrease the number of leads and therefore ease the constraints on platform width and consequently on probe spacing as well.

## 5.3 Foldable Test Structures

While the concept of foldable devices and bendable interconnects is not novel, when applying these ideas to a new application, examination of specification values is essential. The strength of the folded structure, the continuity of the interconnect, the dimensional impact of the radius of curvature due to bending, and stabilization mechanisms all need to be considered. Test structures to investigate the impact of the beam parameters and to explore methods of latching folded probes were made.

### 5.3.1 Beam Bending Layout Test Structures

The main parameters which influence interconnect folding are the material and style (shape) of the bendable leads as well as their length, width, pitch, and number. These parameters were analyzed with two beam-bending test structures, the first of which is illustrated in Fig. 5.8 and detailed in Table 5.1.

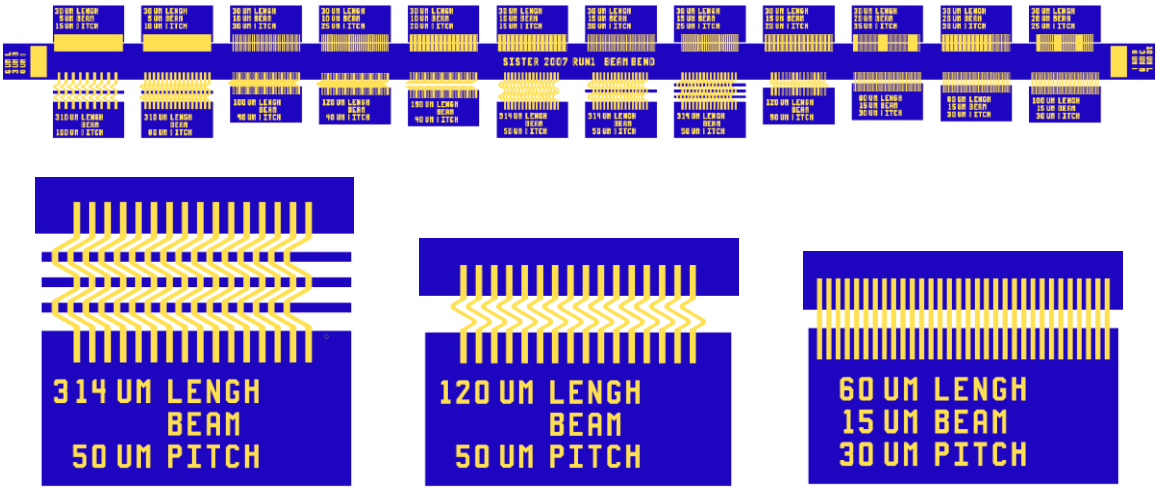



Fig. 5.8: Original beam bending test structure (top) and close-ups of three tabs.

| Table 5.1: Summary of Original Beam Bending Test Structure Parameters | | | | | |
|---|---|---|---|---|---|
| **Design** | **Style** | **Length*** | **Width** | **Pitch** | **Number** |
| **1** | Zigzag A with 3 Bars | 314µm | 12-20µm | 50µm | 16 |
| **2** | Zigzag A with 1 Bar | | | | 16 |
| **3** | Zigzag A | | | | 16 |
| **4** | Zigzag B | 310µm | 17-30µm | 100µm | 9 |
| **5** | | | | 60µm | 16 |
| **6** | Zigzag C | 120µm | 10-20µm | 50µm | 16 |
| **7** | Zigzag A | 150µm | 12-20µm | 40µm | 24 |
| **8** | Zigzag D | 120µm | | | 24 |
| **9** | Zigzag D | 100µm | | | 24 |
| **10** | Straight | 100µm | 15µm | 30µm | 32 |
| **11** | | 80µm | | | 32 |
| **12** | | 60µm | | | 32 |
| **13** | | 30µm | 20µm | 35µm | 27 |
| **14** | | | | 30µm | 32 |
| **15** | | | | 25µm | 32 |
| **16** | | | 15µm | 30µm | 32 |
| **17** | | | | 25µm | 32 |
| **18** | | | | 20µm | 48 |
| **19** | | | 10µm | 30µm | 32 |
| **20** | | | | 25µm | 38 |
| **21** | | | | 20µm | 48 |
| **22** | | | | 15µm | 64 |
| **23** | | | 5µm | 15µm | 65 |
| **24** | | | | 10µm | 96 |
| **25** | | 10µm | 3µm | 6µm | 72 |
| **26** | | 6µm | | | 72 |
| *Indicates span from edge of the silicon tab (back-end) to the edge of the platform. | | | | | |

The original beam bending test structure surveys an array of beam parameters. It consists of a main silicon platform, corresponding to the array platform, with a number of silicon tabs, representing back-ends of probes. The beams connecting the platform and tabs are plated gold; they are not encapsulated. This provides the opportunity to focus on the interconnect parameters independent of the insulation. The other bending test devices also follow this platform and tab structure.

At the end of the process flow, wafers are thinned from the back-side with DRIE and then devices are released in TMAH (tetramethylammonium hydroxide). Full release is essential for folding functionality. Test structure design variations included zigzag shaped beams with and without silicon braces. The zigzag shape follows the design by Yao and was originally implemented since it increases the effective opening for the anisotropic release etch due to the self-limiting V-groove formed by the (111) planes, as pictured in Fig. 5.9 [63]. Straight beam designs were also tested. Since the release is continued until the etch-stop for the boron-doped silicon is reached, and when integrated cables are included then until they are also released, it was determined that straight beams were functional and also have a simpler design.

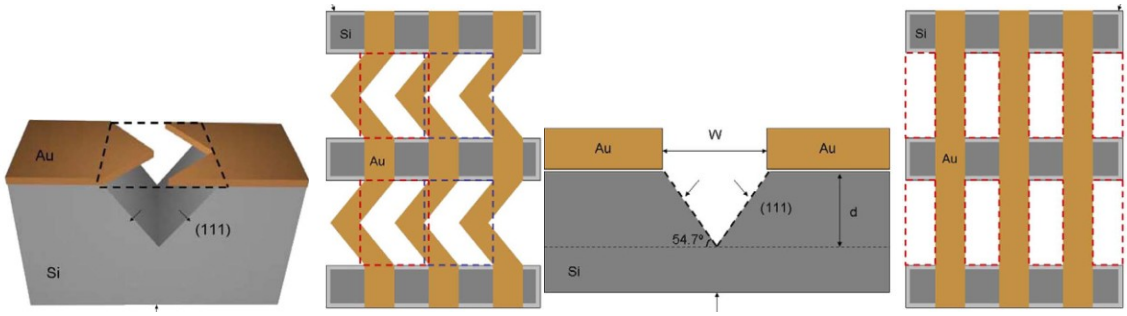



Fig. 5.9: Pictorial representation of effective opening for the release etch with zigzag and straight beams from [63].

The second bending structure focused on the length the beams span from the edge of the silicon platform to the edge of the tab. This parameter influences the accuracy in bend placement and the final position of the tab in relation to the platform. When the space is too small, bending may not be possible due to boron diffusing from the designated silicon regions into the bend region or due to lack in length of beam material which must stretch to form the bend. Two versions of this structure were made, as shown in Fig. 5.10. For both versions, one particular beam width and pitch were selected and

the gap was varied. The first version was not encapsulated. The beam width and pitch were 20µm and 25µm respectively; fourteen spanning length variations are included from 2µm to 50µm. The second version of this test structure utilized 17µm-wide beams at 29µm pitch with twelve length variations from 5µm to 50µm.

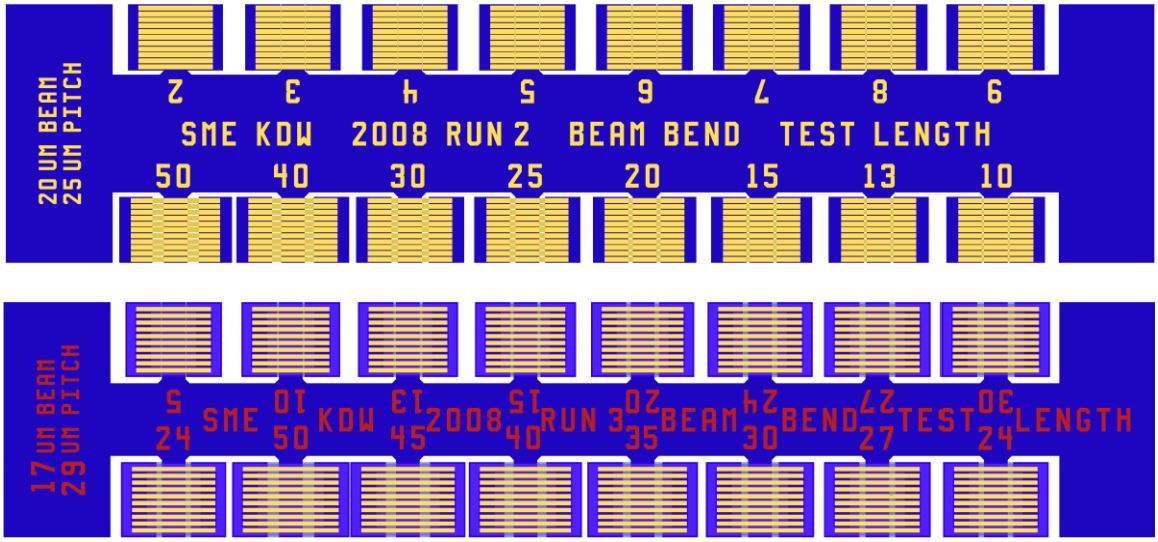



Fig. 5.10: Test structure for beam spanning length without encapsulation (top) and with encapsulation (bottom).

The beam bending test structures were used to examine layout parameters; Fig. 5.11 shows fabricated devices. All of the variations of the beam bending test structure were fully released so bending was possible. It was significantly easier to place the fold along the edge silicon platform (if the interconnect was on the outside of the fold) than it was to fold the beams precisely in the center, as originally intended. Folding both forwards (bringing top sides of the platforms and tabs towards each other) and backwards were considered. Bending with the interconnect on the inside of the fold sometimes caused the beams to peel off of the platform or tab. Repeated bending tests (from approximately $0^o$ to approximately $90^o$) were used to assess the design strength. Most designs (fabricated with 4µm thick plated gold beams) withstood more than twenty such bends. Often, all or most beams on one tab broke at the same bend number; occasionally half broke and then the other half broke after a few more folds. Wider and longer beams withstood more bending, as did the zigzag designs. However, the longer beams were more likely to curve as the tab was brought to the $90^o$ position and shorter beams had a sharper bend. This lack of precision in bending that the zigzag and longer straight

designs had would significantly increase assembly challenges; better jigs would help control bend placement. Due to this observation, the spanning length test structure was designed; results from these devices show they can be divided into three groups. The tabs with the smallest layout gaps (<3µm) had silicon remaining in the gap so bending was impossible. The next group could be bent, but due to the small spacing since the silicon of the tab and platform, the interconnect would tear if over-bent. The last group could successfully be bent, even completely closed, that is bringing the tab flat against the platform. These results assisted in design decisions for the functional FAST prototype.

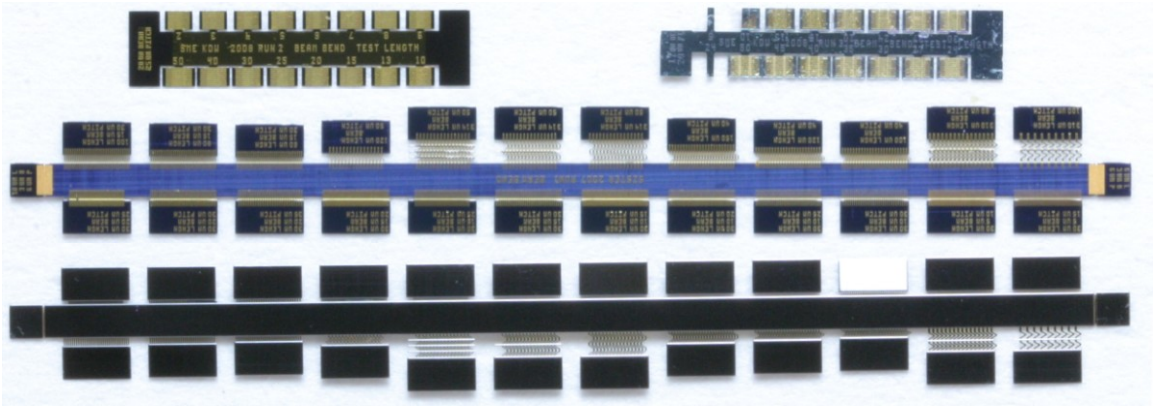


Fig. 5.11: Photograph of fabricated beam bending layout test structures showing the spanning length non-encapsulated (top left) and encapsulated (top right) devices as well as the front (middle) and back (bottom) of the beam bending structure.

### 5.3.2 Interconnect Fabrication Thickness

While the test structures presented above explore factors at the layout level which influence beam bending, fabrication parameters also play a role. In particular, the thickness of the interconnect beams effects durability and final device positioning. One thin sputtered gold layer and three thicknesses (2, 4, and 6µm) of plated gold were evaluated. The 4µm thickness was selected as optimal due to its ease of bending and resilience during repeated bending as well as that during over-bending. The 2µm thick version tore relatively easily and the 6µm version had interconnect liftoff problems. The latter issues may have been caused in part by an overetch during the gold patterning, but it also seemed that the extra beam strength put additional stress on gold-silicon adhesion. Fig. 5.12 shows a 4µm device that was over-bent once; while at the fold the outer surface

appears to have small cracks due to the stretching, the interconnect path is not compromised. Another critical factor is the encapsulation material and thickness. Later structures employ parylene encapsulation to provide a complete foldable interconnect demonstration.

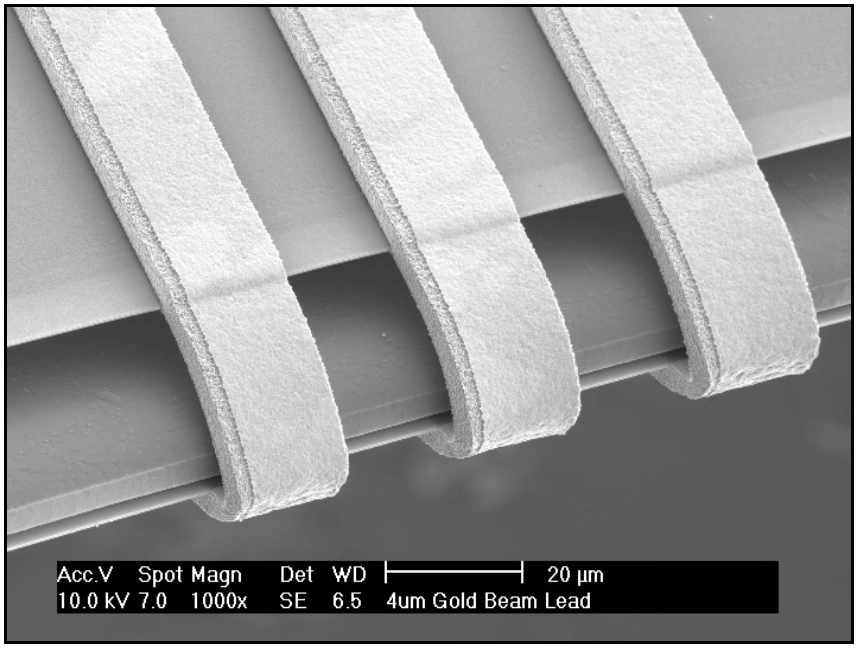



Fig. 5.12: SEM of 4µm thick plated gold interconnects with one-time over-fold illustrating minimal effects of excess bending.

### 5.3.3 Latching Test Structures

Once arrays are folded into position, a latching mechanism is helpful to permanently secure them or temporarily hold them until they are secured with silastic or a similar material. Layouts for four options are illustrated in Fig. 5.13 and Fig. 5.15.

The shank-spacer latching design is integrated off the back-end of one of the outer probes in the array, in between its central shanks; a photograph is shown in Fig. 5.14. The remaining probes have silicon wings on the inside edge of the central shanks. These wings fit into respective notches on the latch. Once folded, the latch should undergird the array and hold each probe with the proper relative spacing. Although this latch design meets the requirement of not significantly increasing the vertical rise, it considerably increases the assembly challenge. In order to fold the latch, movements close and even in between the probe shanks are required; this escalates the opportunities for shank breakage. Therefore, this design was not implemented on the final array.

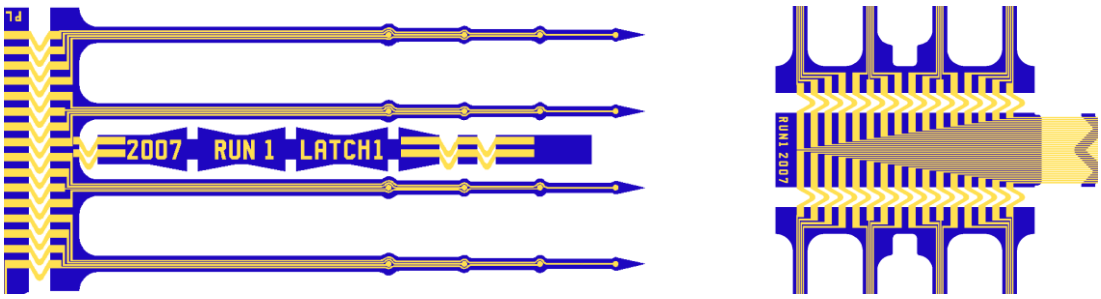



Fig. 5.13: Shank-spacer latch design.

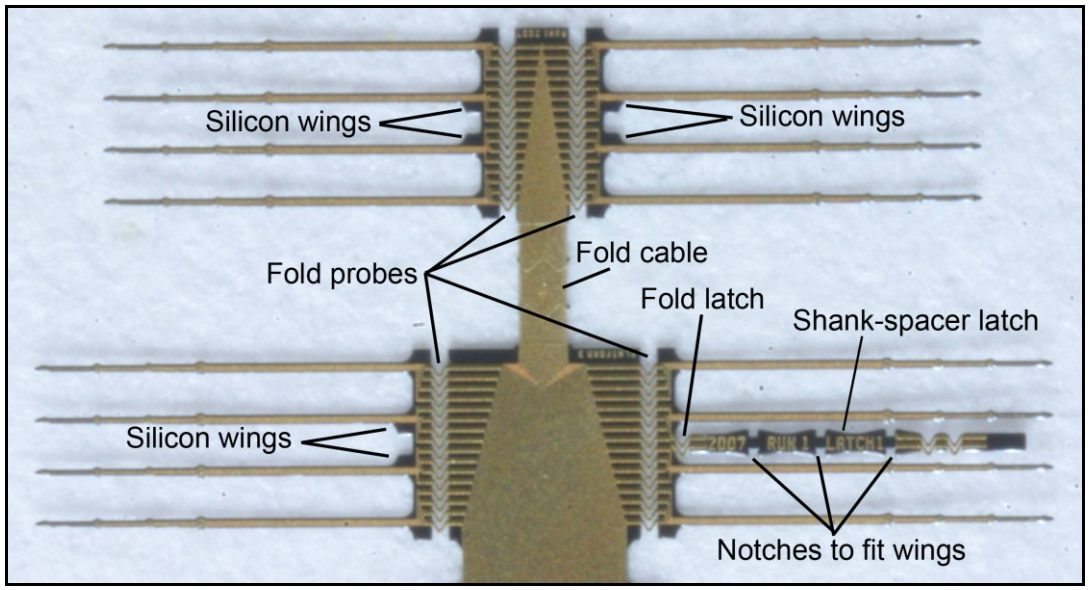



Fig. 5.14: Labeled photograph of the shank-spacer latch design.

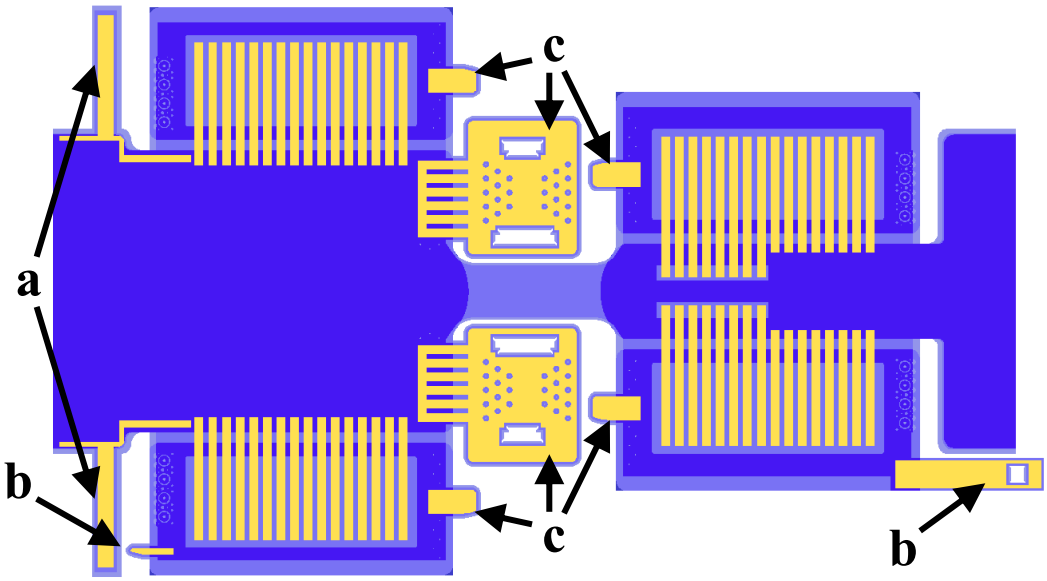



Fig. 5.15: Cable clasp (a), back-end latch (b), and platform gate latch (c) test structures.

The cable clasp latch is intended for arrays in which integrated cables leave both the top and bottom platforms. It consists of a foldable interconnect encased in an encapsulating sheath and protrudes from the top cable near the platform region. Once the bottom platform is placed vertically on top of the top platform, the cable clasps on each side may simply be bent around the bottom cable, as shown in Fig. 5.16, to assist in keeping the two cables aligned and the two platforms in contact. Assembly experience verified the benefit of this structure, especially during the remaining folding steps; wider or additional clasps would improve the design.

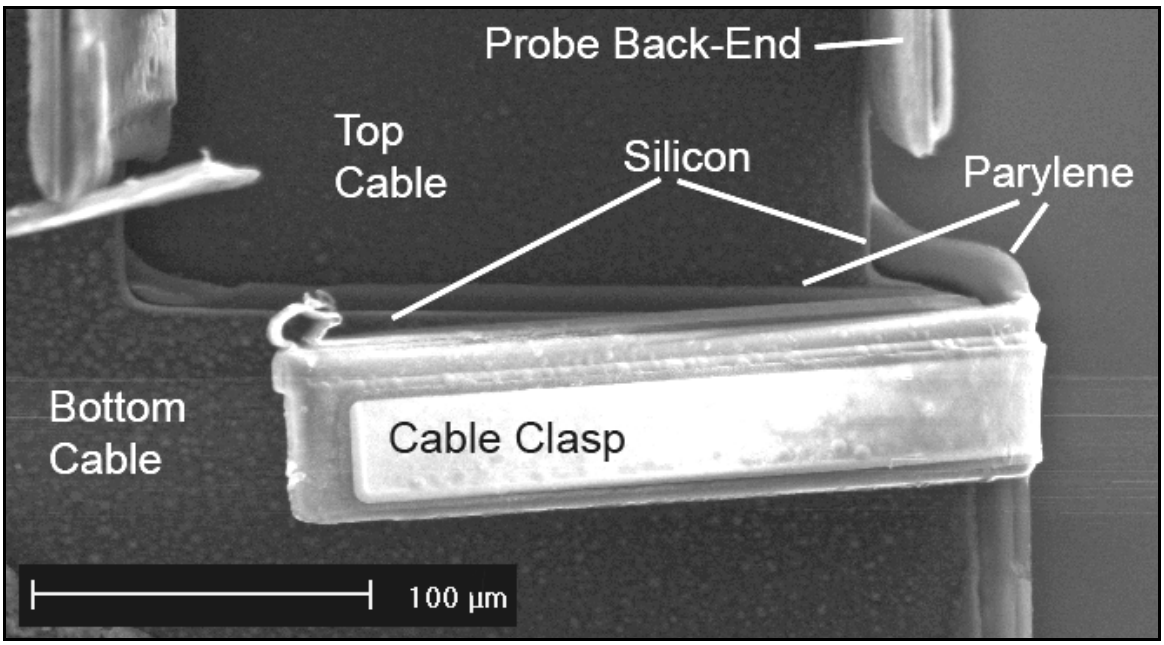



Fig. 5.16: SEM of the folded cable clasp latching the top and bottom cables.

The back-end latch consists of a silicon finger which extends from the back-end of a bottom platform probe and the corresponding latch which is integrated with the back-end of the adjacent top platform probe. After the probes are in their final position, the bendable latch is folded to hook the silicon finger. This design requires revision before successful implementation on an array. Due to the strength of the fabricated gold, and non-supported silicon during the folding, the bending process currently causes the parylene to lift-off the silicon back-end, as shown in Fig. 5.17. Suggested alterations include using thinner gold or less gold width and longer length.

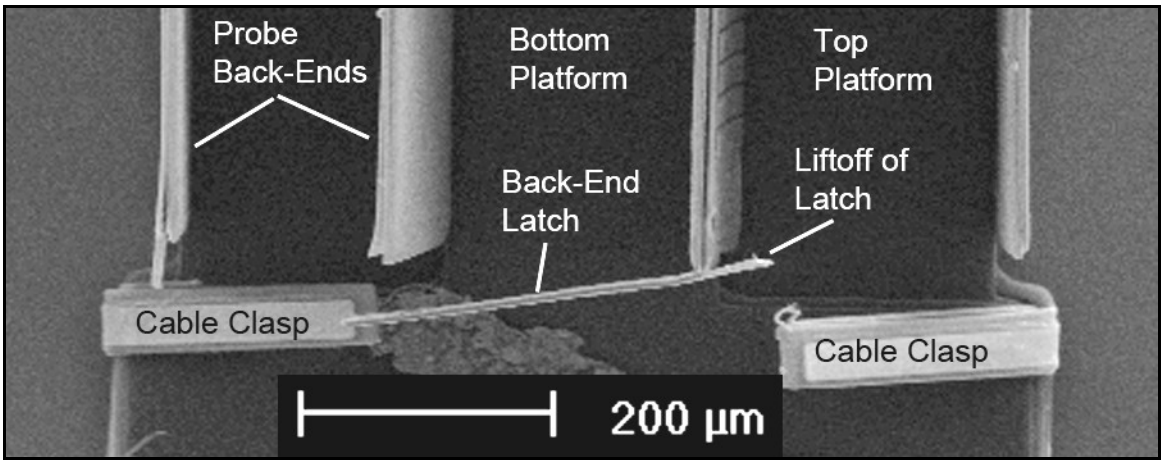



Fig. 5.17: SEM of two folded cable clasp latches and the back-end latch.

The platform gate latch overcomes some of the challenges inherent in the back-end latch. This design comprises silicon fins on all four probe back-ends and foldable gates which are attached to the top platform. Once the probes are in position, the gates are bent upwards, latching the fins, to limit the range of motion of the probes, as shown in Fig. 5.18 and Fig. 5.19. The design of both parts was carefully considered to ensure smooth interlocking during assembly. Since the top platform is pressed against the assembly base during folding, the gate motion does not induce the same risk of parylene-silicon separation that occurs with the back-end latch. Trials with this structure demonstrated its merit especially for the top platform probes. While it also works for the bottom platform probes, more careful assembly is necessary to ensure proper engagement. Further iteration to tighten the tolerances would enhance the design.

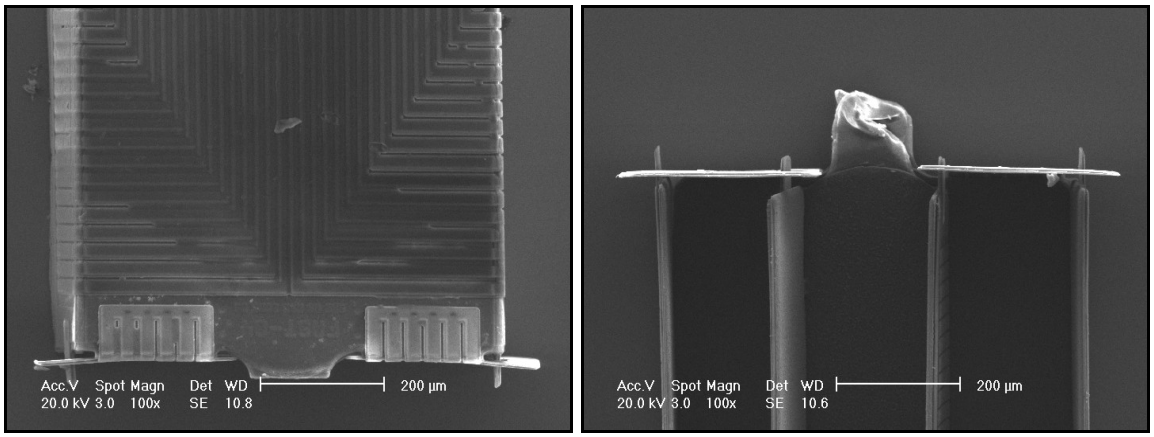



Fig. 5.18: SEMs of the platform gate latch test structure after folding and latching viewed from the top of the top platform (left) and from the bottom (right).

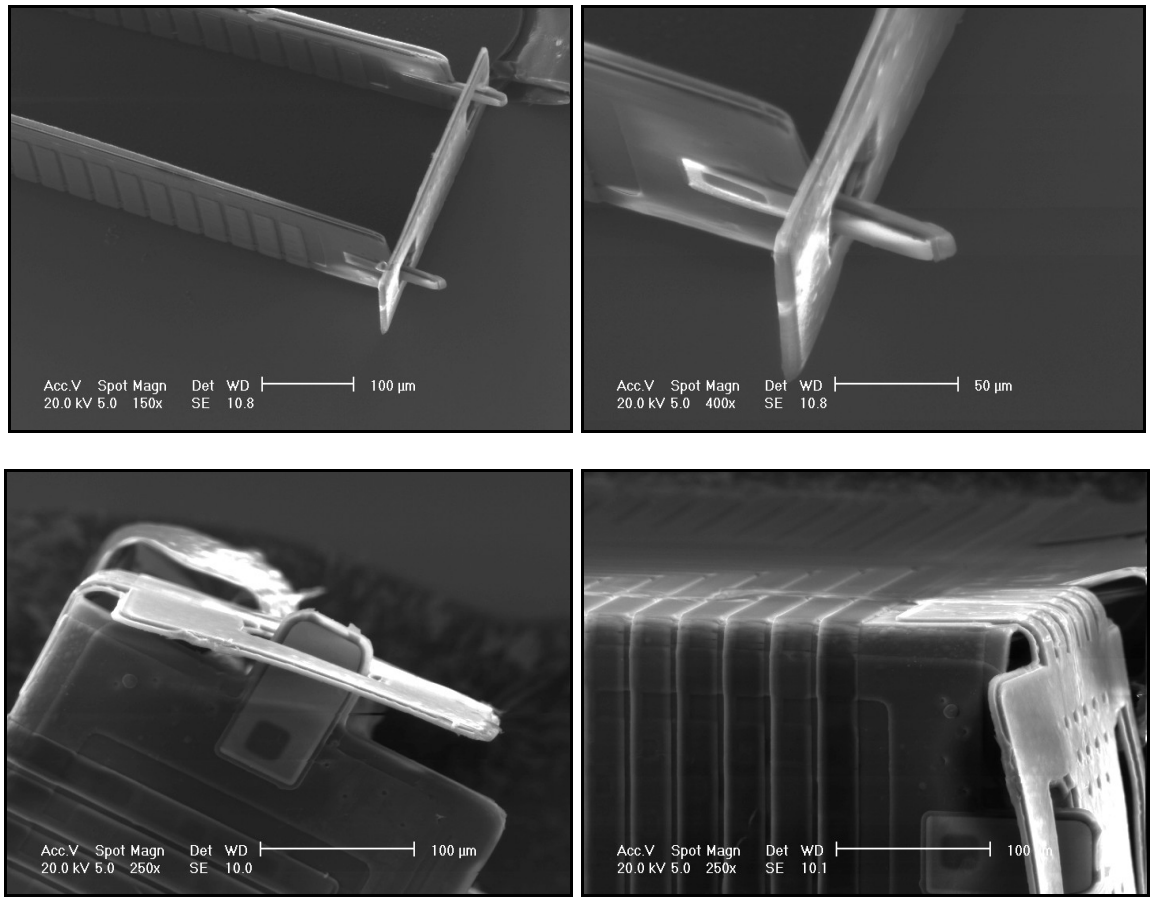



Fig. 5.19: SEMs of the platform gate latch test structure showing the silicon fins in the latch hole with gate fully in place (top) and with partial gate closure (bottom) due to lack of sufficient pre-bending.

The cable clasp and platform gate latches were included on the functional FAST prototype array. After folding, these mechanisms were employed to assist in maintaining desired position until silastic was placed within the platform region to decisively secure the structure. Future latch work should focus on decreasing the tolerances of the gate latch and developing a similar latch for the other back-end edge. The major assembly challenge is aligning the bottom platform to the top platform and achieving a final structure with all of the shanks parallel. This challenge increases as the shank length increases since any intrinsic stress causes a bow in the shanks which is more apparent with longer length and because any misalignment is also magnified with longer shanks.

## 5.4 Proof-of-Concept Devices

Three variations of FAST array designs were fabricated as proof-of-concept devices. These include a two-probe single-platform device and two four-probe dual-platform arrays; the structures do not include latching mechanisms. To reduce processing time and cost, these are dummy devices; all interconnect leads were fabricated using plated gold and the interconnect was not encapsulated. All three structures utilize the design topology in which a single cable leaves the array. Fig. 5.20 shows photographs of these devices prior to assembly.

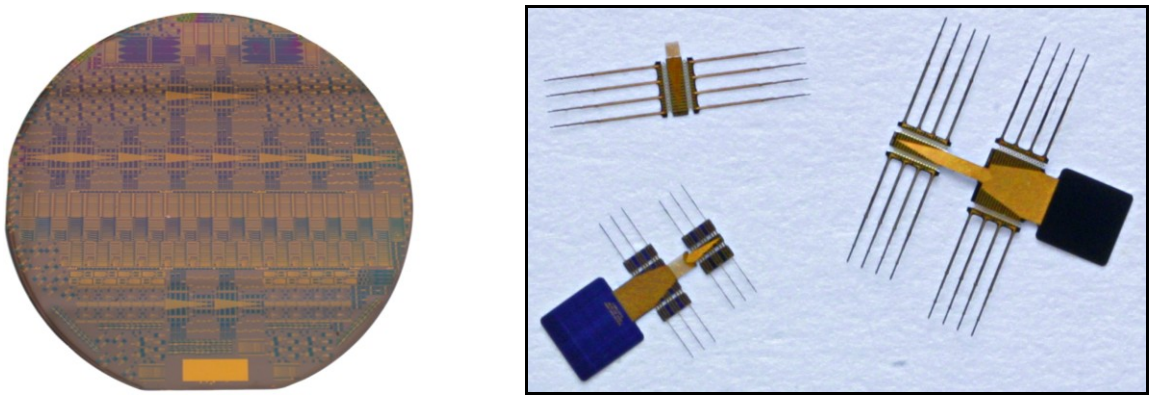


Fig. 5.20: Photos of the proof-of-concept wafer (left) and released arrays (right).

### 5.4.1 Two-Probe Single-Platform Unit for Thirty-Two Sites

The first design consists of two probes and the intervening platform; the layout is illustrated in Fig. 5.21. Each probe in this unit has four shanks with four leads per shank, for a thirty-two site device; the shanks are at a 200µm pitch. The silicon platform is 212µm by 761µm, resulting in a footprint of 0.161mm$^2$. In order to achieve this narrow design, the platform interconnect is at a 6µm pitch. When fully implanted, the array would protrude less than 140µm above the tissue surface.

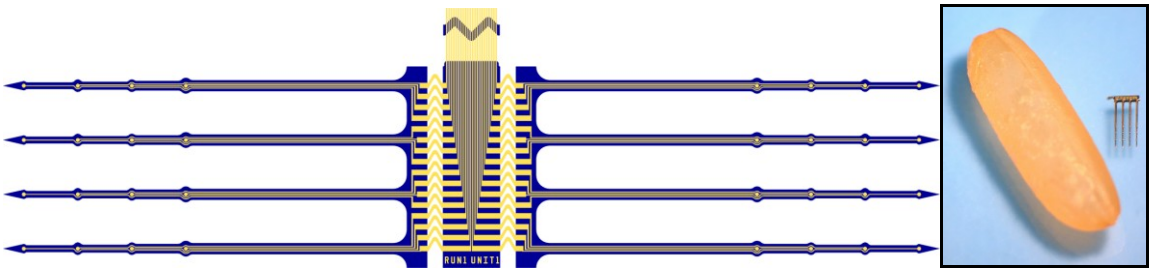


Fig. 5.21: Two-probe FAST unit layout (left) and folded unit with a grain of rice (right).

### 5.4.2 Four-Probe Dual-Platform Structure for Sixty-Four Sites

The second design is comprised of four-probes and two platforms; the layout is shown in Fig. 5.22. The smaller, bottom platform makes use of the two-probe unit design and the top platform has a similar probe structure. The top silicon platform is 752µm by 761µm which forms a 0.562mm$^2$ footprint. The height above the tissue surface would be less than 185µm once fully implanted.

This structure employs zigzag bendable interconnects. It was originally intended that these would be folded at the beam center. However, experimental results show that the preferential folding location is adjacent to the platform as presented in Fig. 5.23. Outer folds are easier to accurately place than inner folds. The thirty-two non-encapsulated leads from the bottom platform join the top platform and all leads exit the array in a single "cable." The fine pitch was determined to be suboptimal since the leads did not stay parallel during folding. These results impacted the design of the functional FAST prototype.

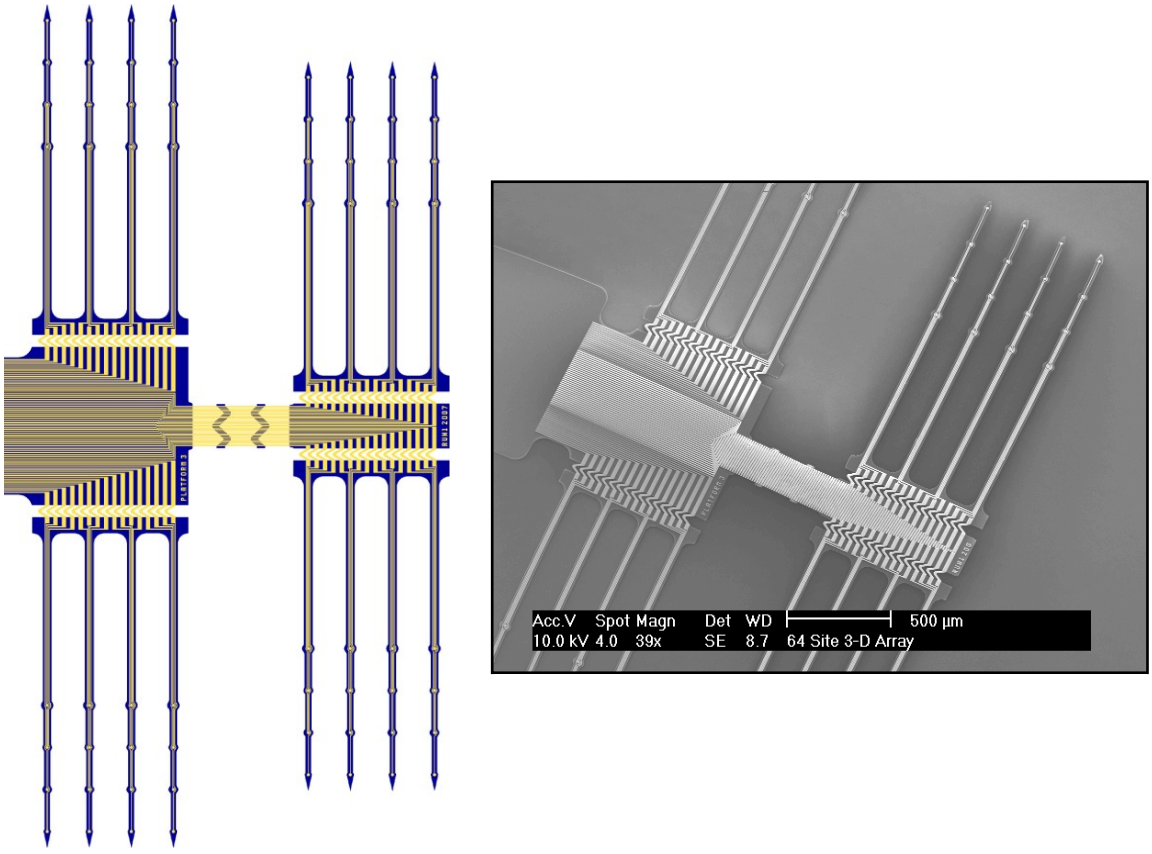



Fig. 5.22: Layout (left) and SEM before assembly (right) of the four-probe FAST unit intended for sixty-four sites.

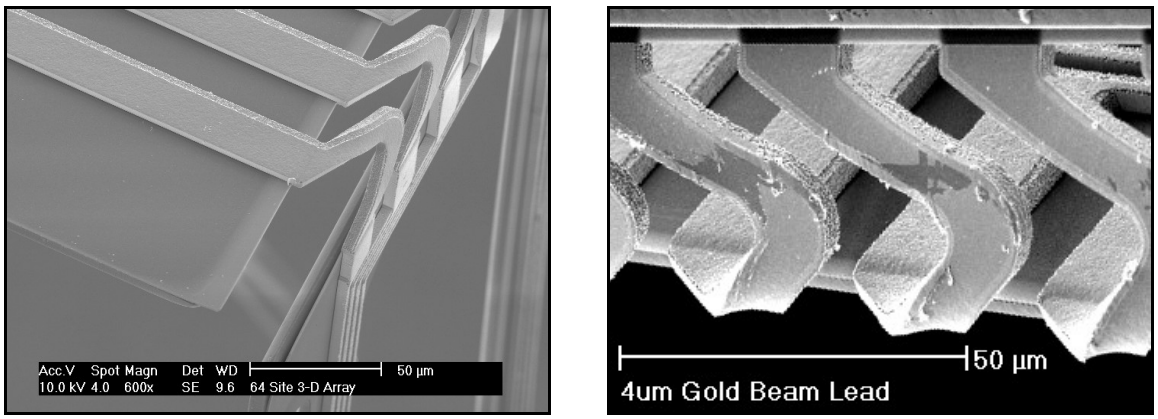



Fig. 5.23: SEM close-ups of outer (left) and inner (right) folds using zigzag bendable interconnects.

### 5.4.3 Four-Probe Dual-Platform Structure for Thirty-Six Sites

The third proof-of-concept structure also consists of four-probes and two platforms; however, there are only three leads per shank and three shanks per probe. The layout is illustrated in Fig. 5.24 and additional images are shown in Fig. 5.25. The top platform of this thirty-six lead device has a 0.369mm$^2$ footprint. The vertical rise is less than 275µm.

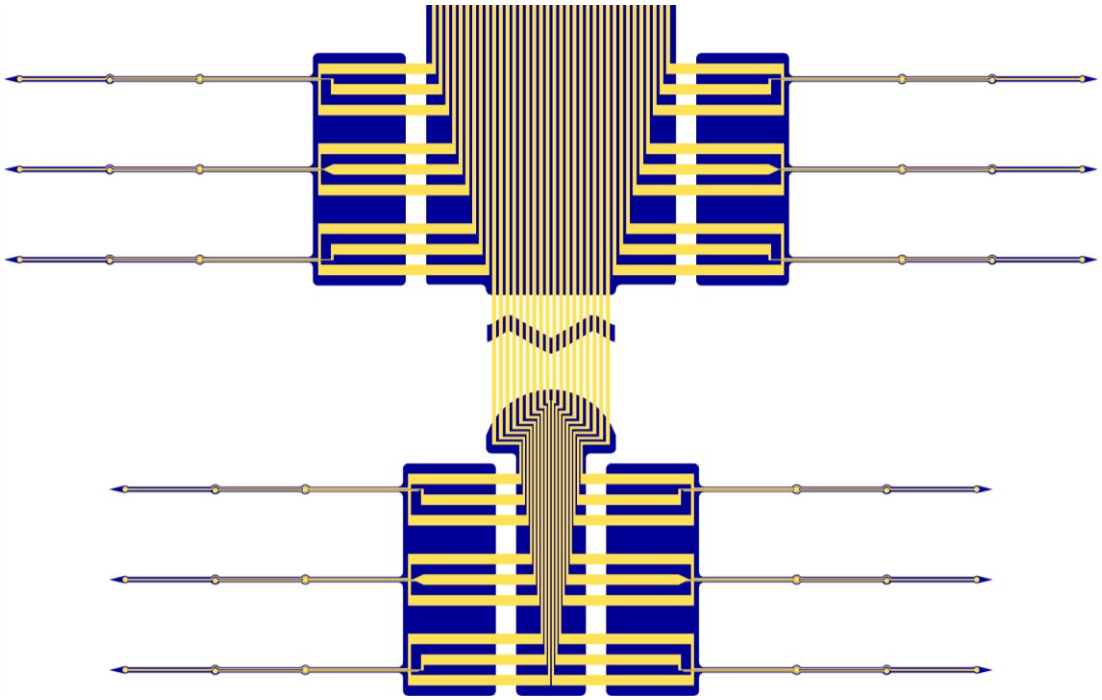


Fig. 5.24: Layout of the four-probe FAST unit intended for thirty-six sites.

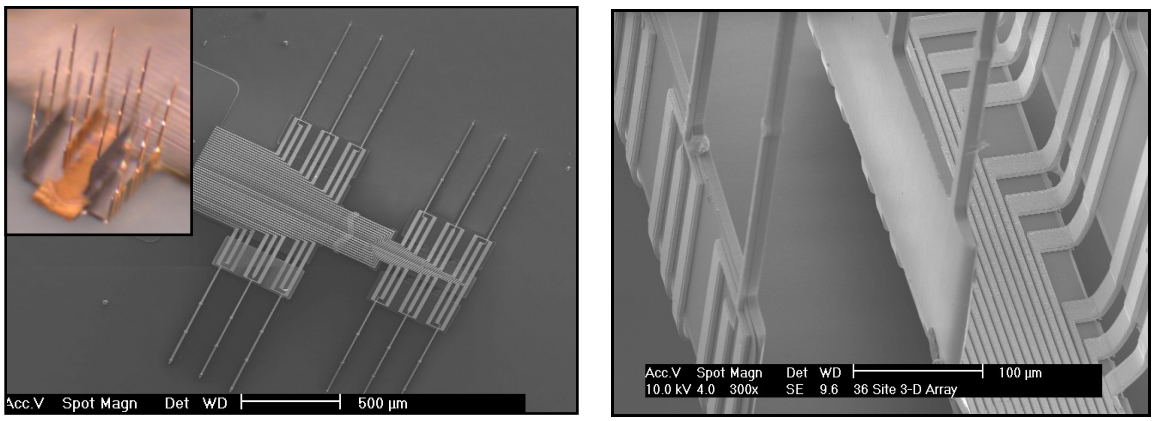



Fig. 5.25: Photograph and SEMs of a thirty-six lead, four-probe, FAST unit.

In order to alleviate the issues that occurred with the fine pitch leads on the platform connector cable of the sixty-four site design, in this structure the bottom platform leads fan out to 7µm beams at a 13µm pitch before they leave the silicon platform. These specifications enable robust interconnects which endure the folding process as shown in Fig. 5.26. Due to the spring effect of the gold leads, it remains difficult to ensure the two platforms are aligned without an intervening gap. This challenge can be overcome by optimizing the cable length and gold thickness. Alternatively, two integrated cables can be employed so that leads leave the top and bottom platforms individually. In this case, the platform connector can consist solely of the encapsulating cable material and is still beneficial in reducing the degrees of freedom during the assembly process.

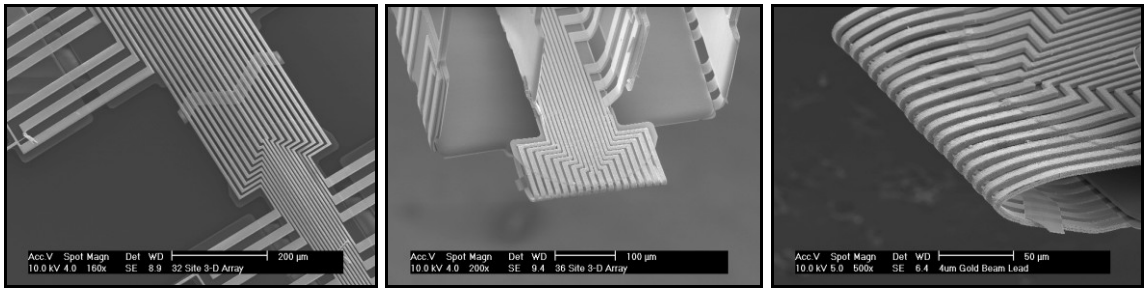



Fig. 5.26: SEM views showing the leads for the platform connector cable.

Outer folds are used with probes attached to the top platform such that the bendable interconnects are on the outside of the fold and the silicon platform and back-end are on the inside, as shown in Fig. 5.27. During the actual folding, the top platform is facedown, with the interconnect towards the assembly surface. While the array is held

in place, slight pressure is exerted on the probe back-end to rotate it upwards. With this fold direction, the platform edge forms a natural demarcation, which, combined with the radius of curvature, determines the bend location.

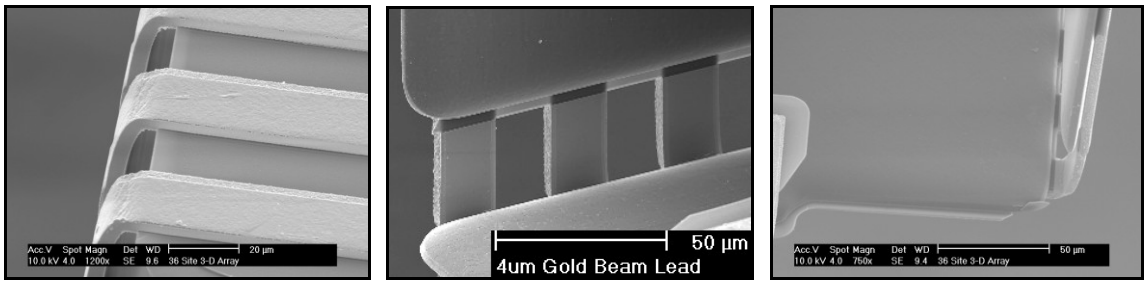



Fig. 5.27: SEM close-ups of outer folds demonstrating the self-alignment along the platform edge.

Inner folds are more challenging than the outer folds to accurately create. If no physical structure is present to govern the bend placement, then separation of the interconnect from the platform may occur as presented in Fig. 5.28. When folding test structures, an assistive device, such as a glass slide, can be used as corner about which to create the fold. With an array, a smaller assembly tool is necessary; an additional silicon platform can be used on top of the integrated platform. However, initial tool to platform alignment and retaining this alignment during the folding are not trivial. Permanently securing an additional platform in place would assist the folding. If high accuracy of these bends is an important design criterion, then an assembly jig for pre-folding may be a preferred approach. Another option, which was pursued for the final design, is to add a twist in the platform connector cable so that both platforms are face down before the probes are folded into position. With this configuration, all of the probe bends are outer folds.

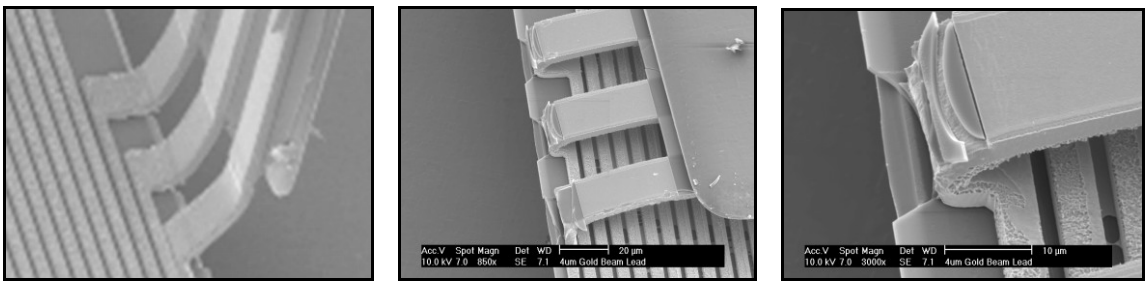


Fig. 5.28: SEMs of forward bends showing inherent challenges.

### 5.5 A 64-Site FAST Array Prototype

In order to further demonstrate the folding architecture, sixty-four site arrays were made using the full fabrication process. The innovative layout enables the standard fourteen-mask 2-D probe process (with integrated cables and beam-lead cable-end option, see Table 6.3) to achieve the 3-D folding structure without process flow modification. The array consists of four, four shank probes, with four electrode sites per 3mm shank, and two integrated cables, one proceeding from each platform. The 177μm$^2$ iridium sites are on 200μm centers along each shank and the shanks are at a 200μm pitch. The array layout is presented in Fig. 5.29 and the three-dimensional structure is illustrated in Fig. 5.30. Table 5.2 compares this design with the proof-of-concept devices described above.

**Table 5.2: Summary of Parameters for Implemented FAST Prototypes**

| | | | Simplified Process | | | Full Process |
|---|---|---|---|---|---|---|
| | | | **A** | **B** | **C** | **D** |
| **Number of Probes** | | | **2-Probe Unit** | **4-Probe Unit** | **4-Probe Unit** | **4-Probe Unit** |
| **Shanks per Probe** | | | 4 | 4 | 3 | 4 |
| **Sites per** | **Shank** | | 4 | 4 | 3 | 4 |
| | **Probe** | | 16 | 16 | 9 | 16 |
| | **Array** | | 32 | 64 | 36 | 64 |
| **Platform / Back-end** | **Top** | **P Width*** | 212μm | 752μm | 485μm | 600μm |
| | | **P Length** | 761μm | 761μm | 770μm | 1033μm |
| | | **P Area** | 0.161mm$^2$ | 0.562mm$^2$ | 0.369mm$^2$ | 0.604mm$^2$ |
| | | **B Height** | 75.5μm | 75.5μm | 180μm | 320μm |
| | **Bottom** | **P Width*** | --- | 212μm | 135μm | 200μm |
| | | **P Length** | --- | 761μm | 593.5μm | 1033μm |
| | | **P Area** | --- | 0.161mm$^2$ | 0.088mm$^2$ | 0.325mm$^2$ |
| | | **B Height** | --- | 75.5μm | 180μm | 300μm |
| **Foldable Leads** | **Style** | | Zigzag | Zigzag | Straight | Straight |
| | **Height (Flat)** | | 58μm | 58μm | 40μm | 24μm |
| | **Width** | | 10-20μm | 10-20μm | 20μm | 17μm |
| | **Pitch** | | 40μm | 40μm | 40μm | 29μm |

*The portion of the platform between the probes.

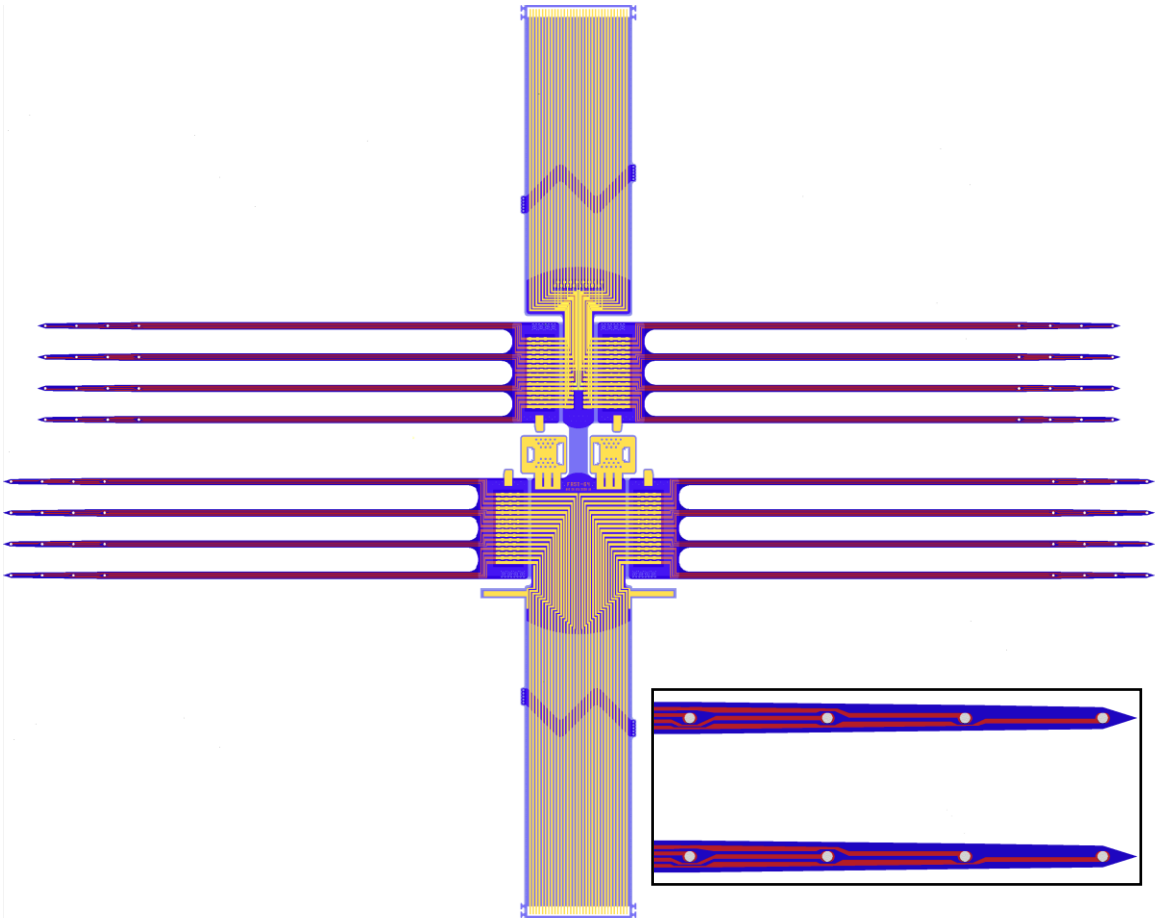


Fig. 5.29: Layout of the 64-site array with inset showing a close-up of the electrode sites on the tips of two adjacent shanks. The FAST assembly method is used to fold the array into the 3-D structure.

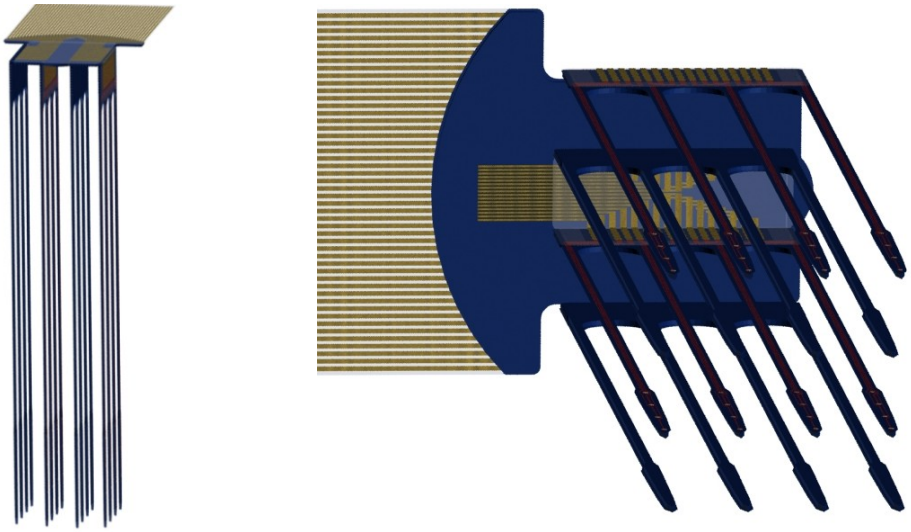


Fig. 5.30: Conceptual drawings of the 64-site folded array. For size reference, note that the shanks are at a 200µm pitch in both directions.

### 5.5.1 Prototype Design

Boron etch-stops enable thin (~12μm substrate) batch-fabricated devices which minimize tissue disruption as calculated in Table 5.3. Polysilicon is used as the conductor along the penetrating shanks. This well-established interconnect allows for the use of high quality LPCVD oxide-nitride-oxide dielectric stacks as insulators on the shanks. In order to keep shank width narrow, the typical nine micron polysilicon pitch on the shank tapers to two micron leads with two micron spaces around the electrode sites. The main shank width of 46μm decreases to 31μm as leads reach their designated site. With a shank thickness of approximately 14.75μm (including the dielectrics, interconnects, and sites) the main shank cross-sectional area is 678.5μm$^2$. When considering a recording range of 100μm from a site, the instrumented tissue cross-sectional area is 0.64mm$^2$. This indicates that the array only occupies 1.7% of the instrumented area. Future designs can further decrease the shank width and thickness by modifying the layout and boron doping to achieve even smaller percentages.

On the probe back-end, leads are transferred to a gold interconnect in parylene encapsulation in order to form the flexible interconnect. Advantage was taken of the 320μm tall prototype back-ends by incorporating triple poly-gold contacts, as shown in Fig. 5.31. This height is not essential and can be reduced by more than half with single contacts; even with this height, the array realizes the lowest-profile ever reported for such a device. The parylene target thicknesses were two and three microns for the bottom and top layers respectively. Three options for the foldable interconnect were considered: all leads plated gold, alternating leads plated or sputtered, and all leads sputtered. The first two options were fabricated on full arrays and the third was fabricated on test platforms.

Parylene encapsulated gold (10μm lead width at 17μm pitch) is used for the top platform routing for design simplicity and lower resistance. While thirty-two leads traverse each platform, in order to have approximately 200μm probe pitch, the bottom platform is only one third of the width of the top platform. This necessitates multi-level interconnect. The process flow opportunely includes not only the polysilicon and cable leads interconnect layers, but also a sputtered gold layer which is typically only used for bond pads and within the poly-gold contacts. On the bottom platform, this layer provides an additional metal interconnect, as illustrated in Fig. 5.32. The dielectric stack isolates it

from the silicon platform and any polysilicon lines and the bottom parylene layer separates it from the cable leads. Any concern about complete encapsulation of this layer can be alleviated with a drop of medical-grade silicone (silastic) during the assembly. After the fold, the sixteen leads closest to the cable remain in parylene encapsulated gold with a 6μm lead width at 10μm pitch. The other half run in either polysilicon or sputtered gold with the same spacing. These leads transfer to the cable-level of interconnect at the mushroom-shaped cable-base.

| **Table 5.3: 64-Site FAST 3-D Electrode Array Specifications** | |
|---|---|
| Instrumented Tissue Volume (assumes 100μm site range) | 800μm x 800μm x 800μm |
| Instrumented Tissue Cross-Sectional Area (assumes 100μm site range) | 640,000μm$^2$ |
| Probe Back-end Width | 646μm |
| Site Area | 177μm$^2$ |
| Site Pitch | 200μm |
| Shank Pitch | 200μm |
| Shank Length (to center of tip-most site) | 3000μm |
| Tip to First Site Distance | 50μm |
| Estimated Shank Thickness (including dielectrics, interconnect, and sites) | 14.75μm* |
| Minimum Shank Width (at center of tip-most site) | 31μm |
| Main Shank Width | 46μm |
| Main Shank Cross-Sectional Area (46μm x 14.75μm) | 678.5μm$^2$ |
| Main Array Cross-Sectional Area (16 shanks) | 10,856μm$^2$ |
| **Main Array Cross-Section as Percentage of Instrumented Tissue Cross-Section** | **1.70%** |
| Shank Layout Area (16 shanks) | 2,177,176μm$^2$ |
| Implanted Volume (16 shanks) | 32,113,346μm$^3$ |
| Penetrated/Instrumented Tissue Volume (800μm x 800μm x 3100μm) | 1,984,000,000μm$^3$ |
| **Implanted Array Volume as Percentage of Tissue Volume** | **1.62%** |
| * See Table 6.3. | |

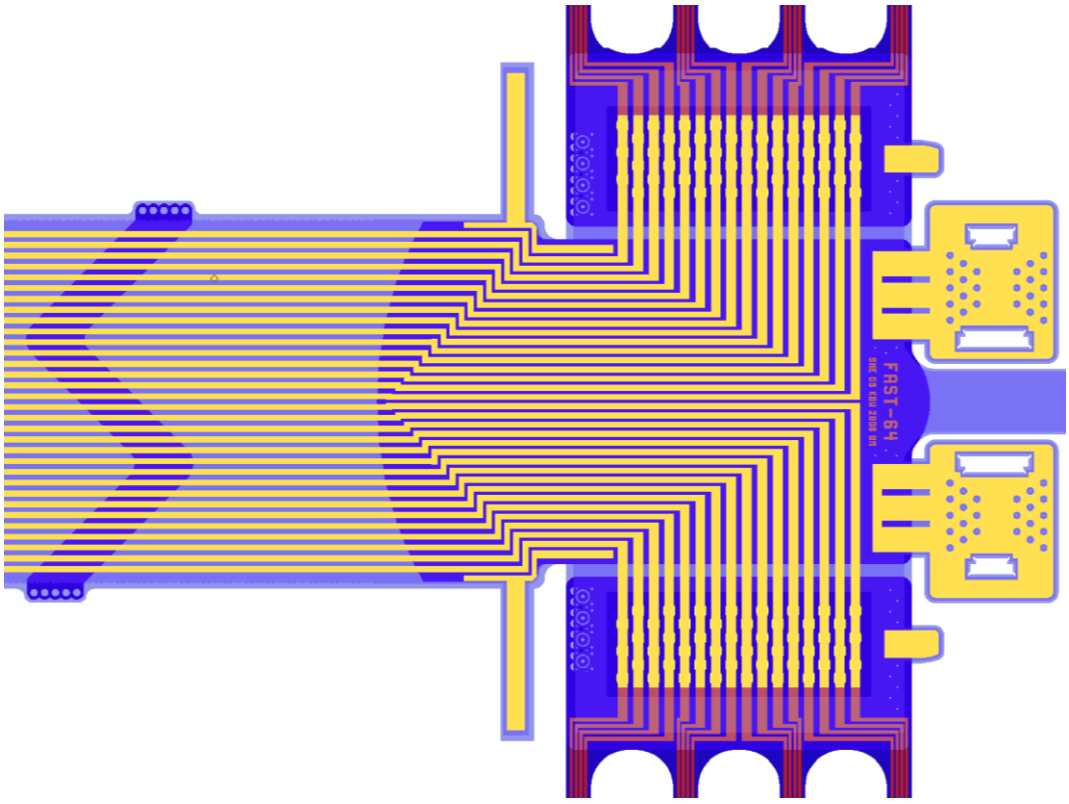



Fig. 5.31: Top platform layout and probe back-ends with triple poly-gold contacts.

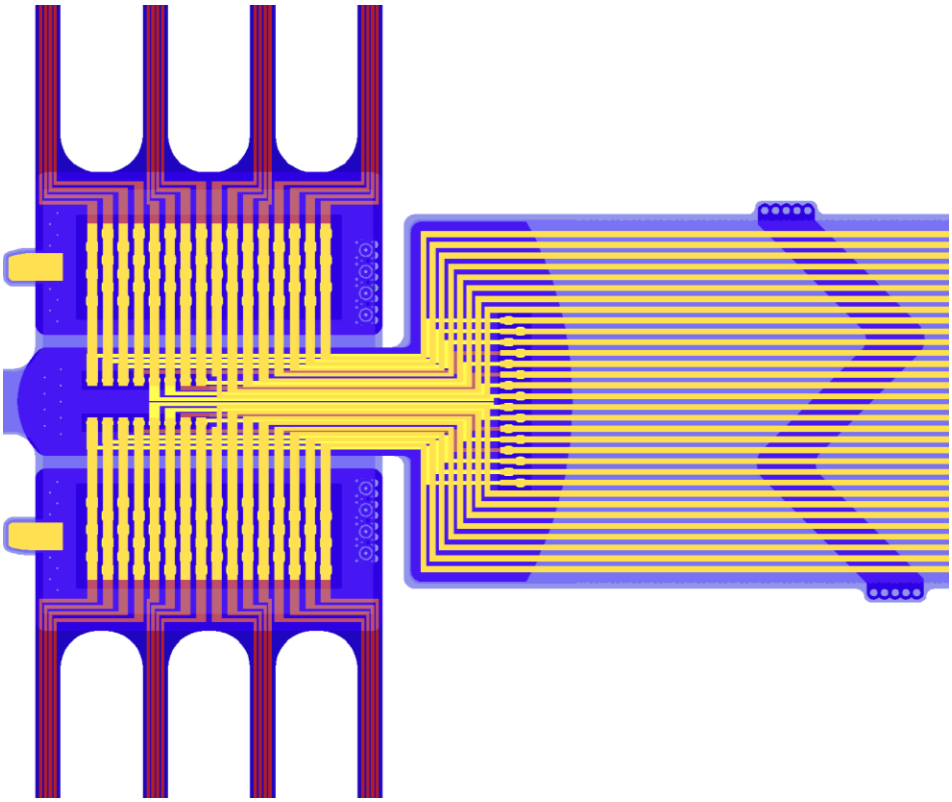


Fig. 5.32: Probe back-ends and bottom platform layout with three interconnect levels.

As detailed above, one of the advantages of the FAST method is that no connections between the probes and the platform need to be bonded after release. On this prototype, two integrated cables are included and no leads cross the platform connector cable. Once assembled, the cables with leads are aligned directly on top of each other thus forming "natural" multi-level interconnect. The cables utilize the same design as the 2-D VCN-DCN cables in Section 6.1.3 with 20µm lead pitch, 692µm main width, and 742µm width across the zigzag anchor. The prototype cables end in beam-leads at the same pitch as the cable leads. Connecting to these proved exceedingly challenging; it is recommended that future designs employ standard bond pad regions (as do the VCN-DCN cables) or fan-out to wider pitch beam-leads. Short cables were included in this design, as Fig. 5.33 presents, but the length could be increased as application requires. Fig. 5.34 displays a close-up of a fabricated device showing the cables leaving the platforms; for this structure, alternating foldable interconnects were plated gold, and remaining lead transfers as well as the cable lines were sputtered gold.

### 5.5.2 Prototype Assembly

Various jigging and assembly tools were considered during the proof-of-concept phase. While the device must be held securely, uneven pressure on silicon components can cause fracture. At the same time, the tool with which the bending is accomplished must be able to be positioned at the appropriate location. A simple and effective means of securing the device while maintaining accessibility for assembly tools was devised by forming an assembly box. This box consists of a metal support base, foam cushion, and latex cover. The device is placed on the box and is held by applying slight pressure with a glass microscope coverslip or slide. The glass pane uniformly distributes pressure, thus holding the device without causing fractures. The foam layer is the key to enabling successful assembly. While securely holding the device, the folding tool can slide under the probe back-end since the foam locally depresses with slight force at the tool tip. Typical assembly tools are a single side of fine tip tweezers and pulled glass pipettes. The latex cover forms a clean surface on which assembly may take place by isolating the array from the foam, which tends to leave particulates on the microstructure if in direct contact and which has precarious holes in which shank tips easily get caught.

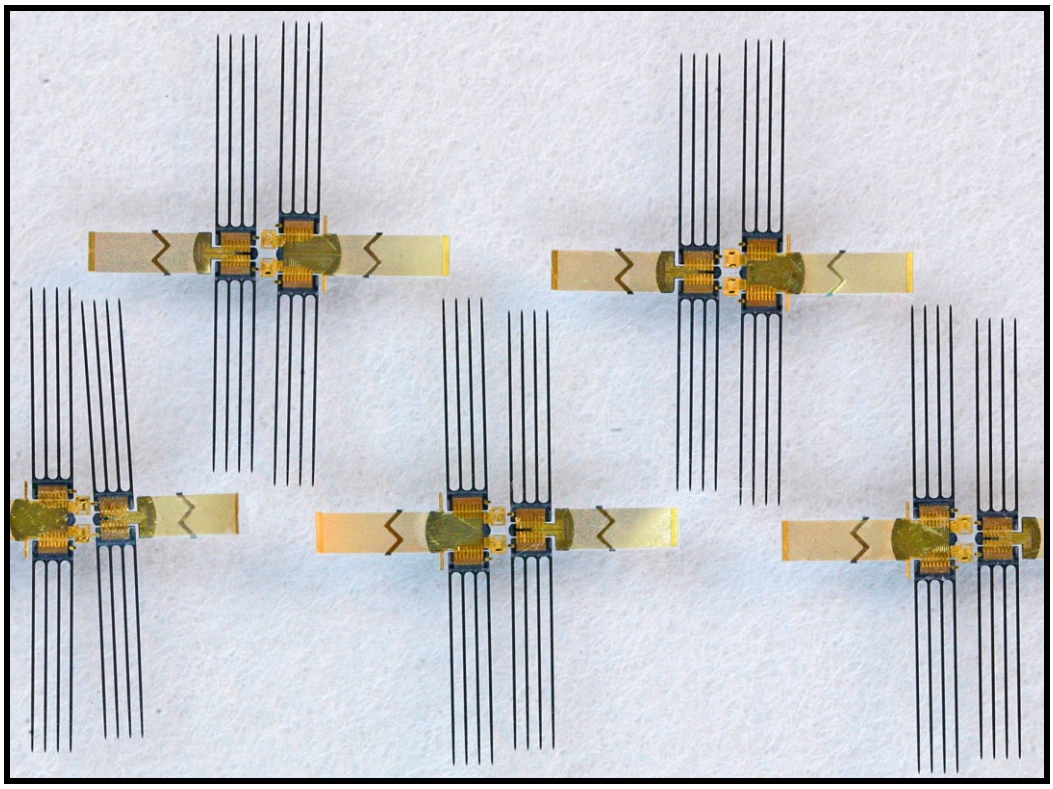


Fig. 5.33: Photograph of five FAST devices prior to assembly.

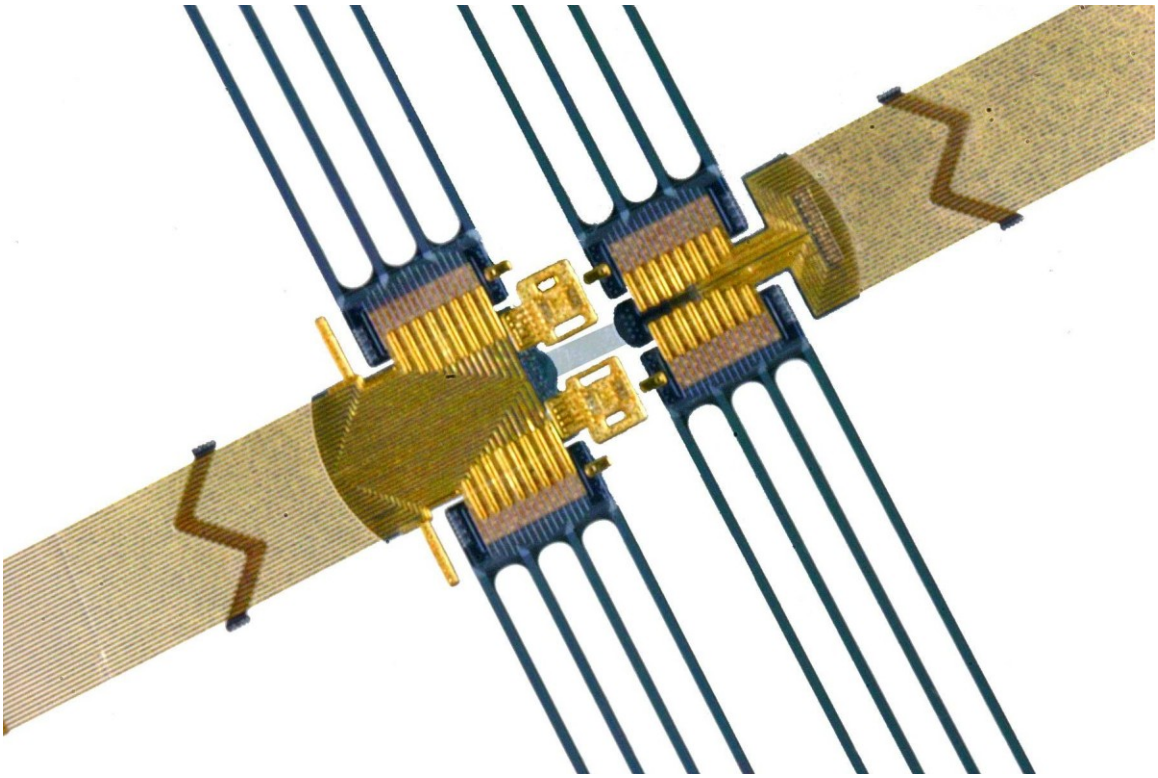


Fig. 5.34: Close-up photograph of a FAST device prior to assembly with background removed from the photograph.

The basic FAST assembly steps were employed with minor modifications based on experience from the proof-of-concept devices, test structures, and initial prototype assembly. The general procedure is photographically illustrated in Fig. 5.35. Assembly occurs "upside down" with shanks pointing upwards after the bending is complete; thus, what is actually the top platform is on the bottom of the assembly stack. After inspecting the front-side for fabrication anomalies, the array is turned face down. The device is held with a glass coverslip over the larger top platform and its cable. Then the platform latches (and probes) are pre-bent more than ninety degrees and partially unbent; this eases the final bending during the securing step. The glass pane is eased back to hold only part of the top cable, removing it from the vicinity of motion in the subsequent step.

The next goal is to place the two platforms on top of each other, both face down. This direction was chosen so the platform edges delineate the bend locations and also because it reduces the risk of the parylene peeling off of the silicon. The assembly tool is used to fold the smaller bottom platform and its cable over the top platform. At this stage the top platform is face down but the bottom platform is face up. In order to form the necessary twist in the platform connector cable, the bottom platform is then guided in a semicircle around to its original position, still face up. Once again, the bottom platform is folded on top of the top platform; both are now face down.

Probe positioning is the subsequent step. The glass pane is used to hold the two platforms, adjacent to the bottom platform folding edge for the first two bends, and then over the silicon extension. These mushroom-shaped projections are advantageous for holding the array since they form one piece with the central portion of the platforms and do not bend as the cables can when folding force is applied to the array. The four probes are individually bent upwards; initial over-bending assists in achieving the final desired angle. The back-ends connected to the bottom platform are designed shorter than those attached to the top platform to compensate for the platform thickness. At this stage, the two platforms are aligned and the cable clamp latches are folded over. Then the assembly box is rotated so that the angle of the probes with the platforms is visible. After fine-tuning the probe angles, the platform latches are moved into position. Silastic is placed in the trenches formed by the platforms and probe back-ends to finalize the angle and further encapsulate the device. This is done simply with the small tip of a pulled

glass pipette; surface tension assists in drawing the adhesive into the trench; filled trenches are shown in Fig. 5.36. SEMs of folded beams are presented in Fig. 5.37. The assembly has taken less than twenty-five minutes; a folded device is shown in Fig. 5.38. After the silastic is cured in the oven, the array is bonded and is then ready for *in vitro* testing and *in vivo* use.

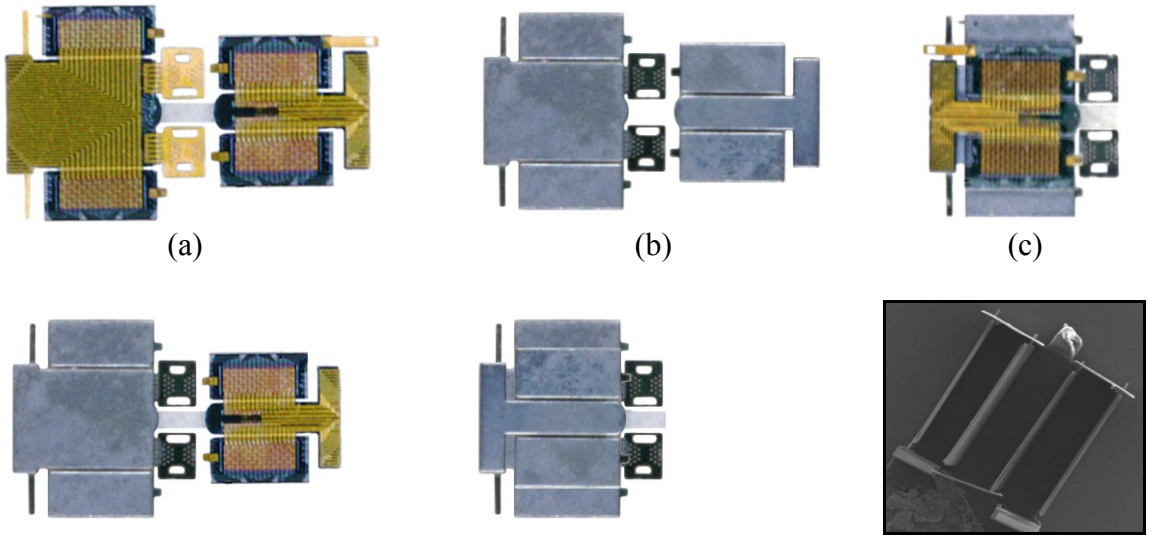



Fig. 5.35: Simplified FAST assembly steps illustrated with latch test structures which were designed without probe shanks: a) top view of the structure showing bendable gold interconnects and parylene intermediary cable, b) bottom view, c) first fold in assembly process, d) after rotation of smaller bottom platform, e) second fold and platform alignment, e) remaining folds of the probes and the cable clamps and platform gate latches.

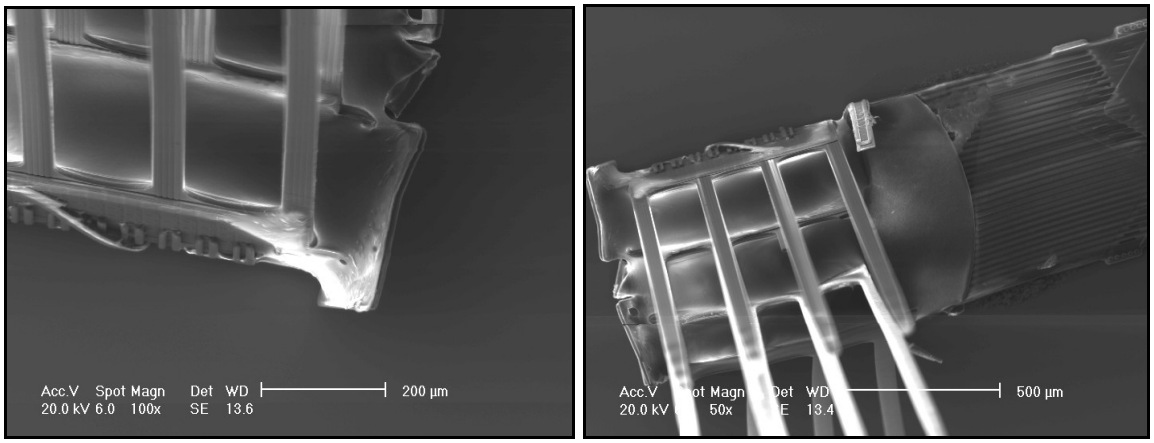



Fig. 5.36: SEMs of a folded array showing the trenches filled with silastic (left) and angled view of the assembled device (right).

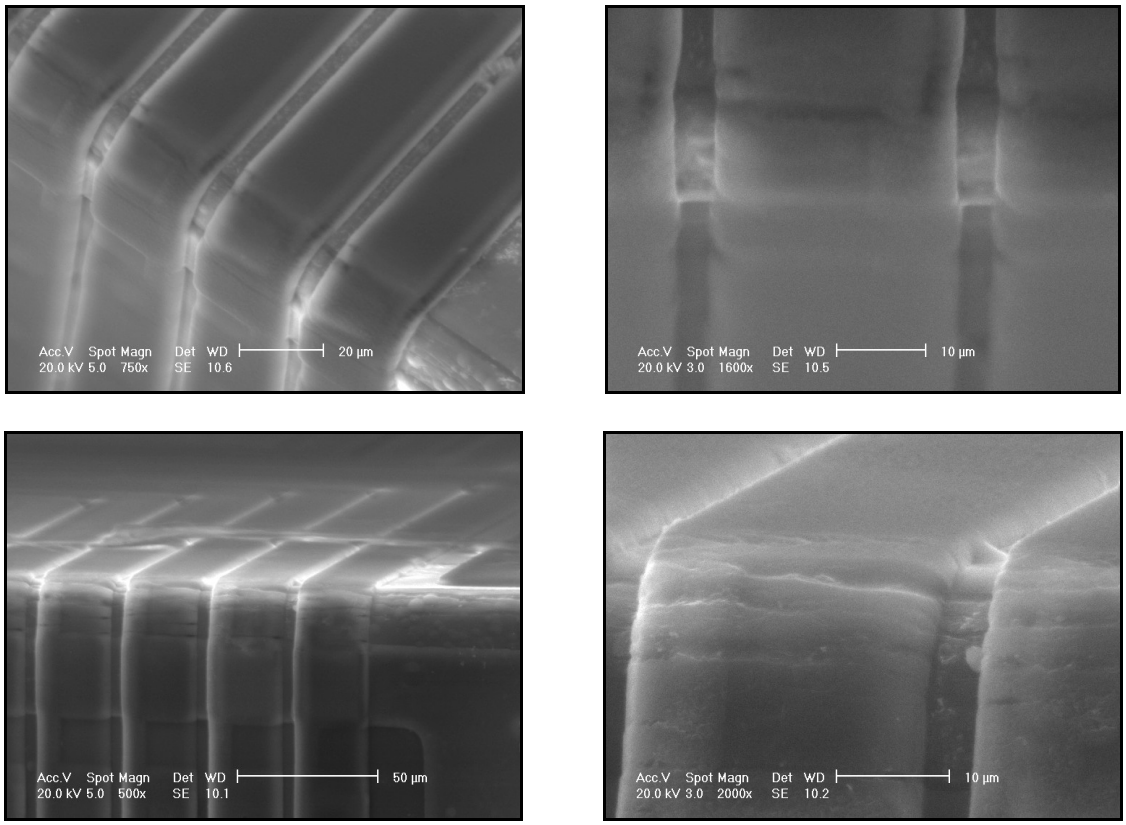



Fig. 5.37: SEMs close-ups of the parylene encased plated-gold interconnects after folding showing traces without (top) and with (bottom) signs of cracking.

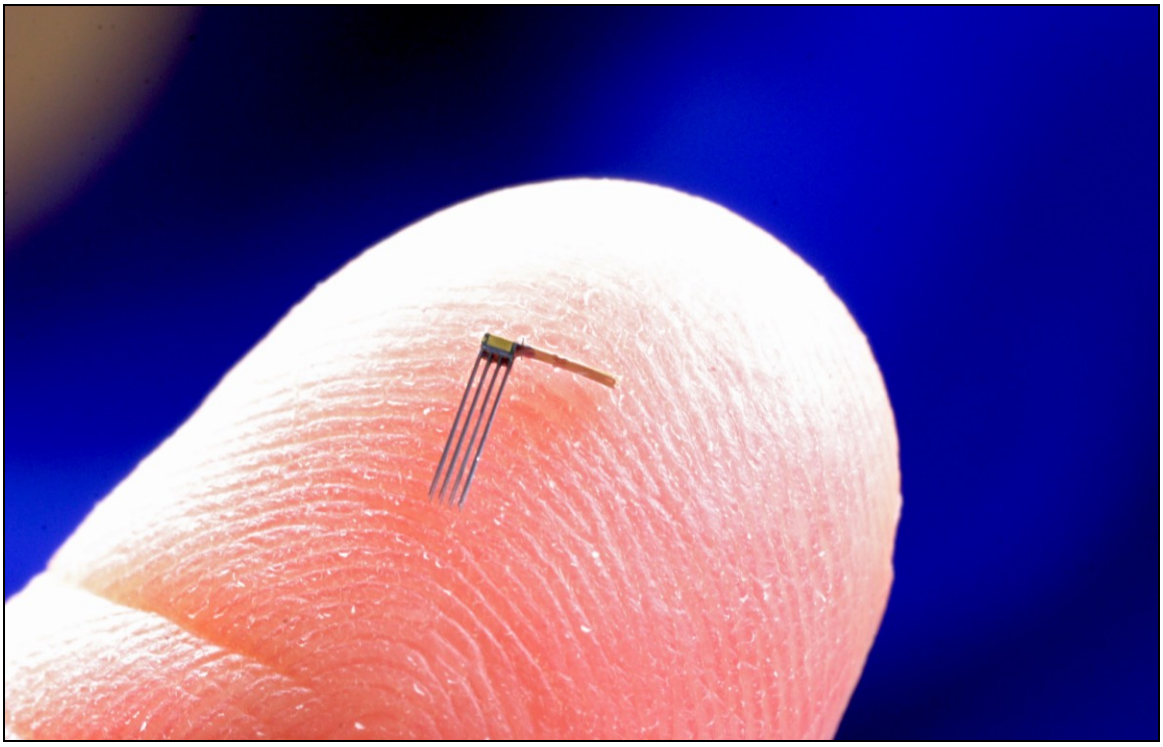


Fig. 5.38: Folded array on a fingertip.

### 5.5.3 *In Vivo* Results

The folded array structure was implanted in the auditory cortex of a guinea pig, as shown in Fig. 5.39, to validate its ability to achieve *in vivo* recordings. The array was mounted on the printed circuit board (PCB) probe-stalk to bring the leads to the headstage of the recording system. Acoustic noise bursts were used to obtain elicited responses. Fig. 5.40 shows acquired peristimulus time histograms (PSTHs) of spike count for four channels; the PSTHs exhibit the expected response pattern for this acoustic stimulus.

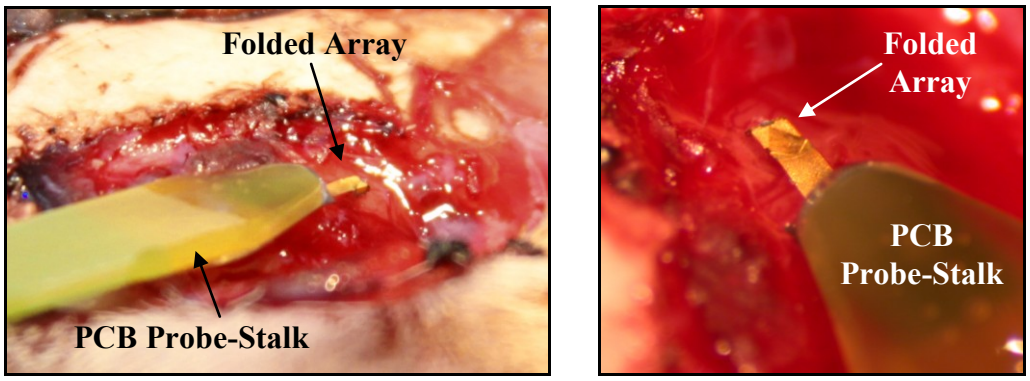



Fig. 5.39: In vivo implantation of a FAST array in the auditory cortex of a guinea pig.

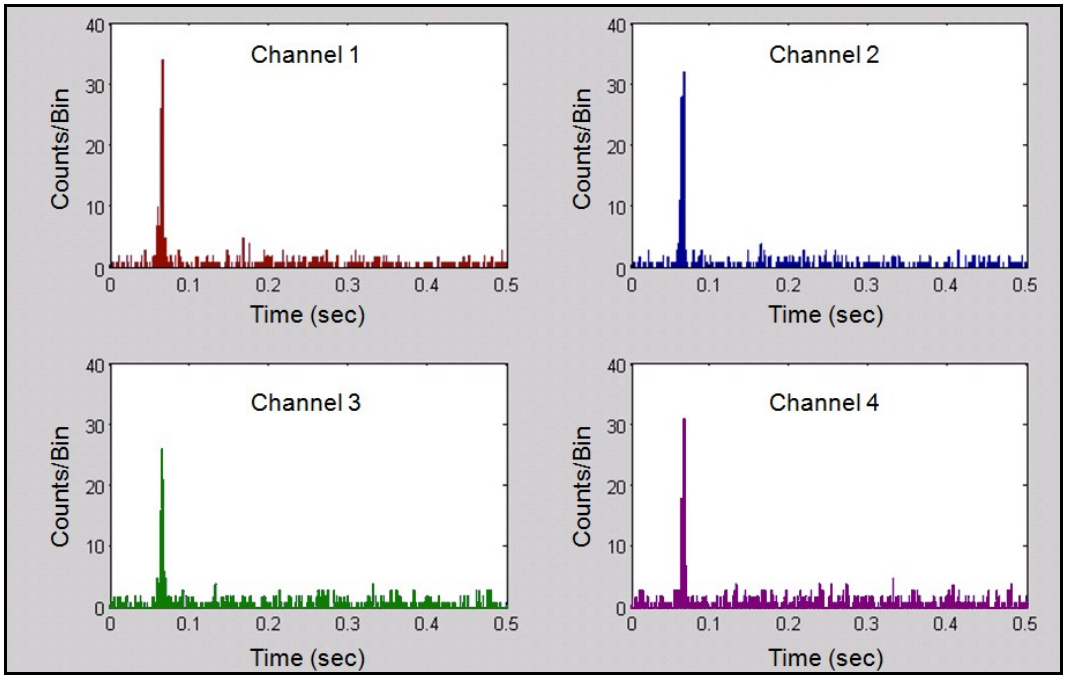



Fig. 5.40: Peristimulus time histograms (PSTHs) of spike count for four channels of the FAST array based on *in vivo* recordings of elicited responses to acoustic noise bursts (onset time = 0.05s) in the auditory cortex of a guinea pig.

## 5.6 Comments on Design Enhancements

While the 3-D folding device demonstrated *in vivo* recording ability, certain aspects of the design can be improved to alleviate challenges in the assembly. The main difficulty was the issue of parylene-silicon adhesion. Arranging the device so that the interconnects were on the outsides of the folds partially reduced the potential for this to occur. Revisions in the layout, such as greater silicon-parylene overlap area and additional silicon anchor "snap" holes, as well as fabrication advances would increase assembly yield. In order to achieve parallel probe alignment, manual adjustments were required to fine-tune probe positioning even after latching the device. The latches should therefore be optimized so that they securely hold the probes at $90^{o}$ to the platform without requiring additional adjustments before the silastic trench-fill. This version of the device used high-density (20μm) beam-lead terminations on the cables; however, significant bonding challenges were encountered. Until fine-pitch beam-lead bonding is optimized, the more robust traditional bond pad design for wire-bonding should be used instead.

## 5.7 Conclusions

Revolutionary advances in neuroscience are being enabled by planar two-dimensional electrode arrays fabricated using silicon micromachining technology. Such arrays are becoming widely used for the high-density stimulation and recording of neural activity; however, they are limited to two-dimensional site placements. Although some three-dimensional arrays have been reported, their availability to the neuroscience community has been limited, in part due to large platform sizes and/or difficult microassembly operations. Three-dimensional arrays are needed that are batch fabricated using high-yield planar processes, can be rapidly assembled, have minimum rise above the cortical surface (allowing dura replacement in chronic situations), and have shank sizes that approach cellular dimensions. This work describes a folding probe design that meets these requirements. The design uses only one additional mask to enable a folded three-dimensional structure using a standard chronic two-dimensional probe process. The process is compatible with the formation of signal processing electronics on the platforms to boost signal levels and minimize output lead counts by multiplexing. Three levels of interconnect with a 10μm minimum pitch are utilized for the thirty-two leads

which traverse each platform. The lateral dimensions of the array are no larger than the area being instrumented; the platform silicon footprint is 0.604mm$^2$. The resulting devices have the smallest platform footprint and lowest profile ever reported and can be formed rapidly from a single microfabricated structure. With a shank thickness of 14.75μm, the present array only displaces about 1.7% of the 0.64mm$^2$ instrumented tissue area. Successful *in vivo* recordings have been achieved.

# CHAPTER VI

# APPLICATION-SPECIFIC 3-D ELECTRODE ARRAY DEVELOPMENT FOR NEURAL MAPPING IN THE GUINEA PIG COCHLEAR NUCLEUS

Advances in neuroscience depend upon the availability of supporting technology for the high-density stimulation and recording of neural activity. While electrode arrays are highly versatile, individual neuroscience applications may require particular array specifications for optimal performance. One such research focus is the cochlear nucleus (CN) of the auditory pathway. The location of the CN within the brain and its surgical approach give rise to substantial constraints which are better met with an application-specific design. To facilitate acute studies, a three-dimensional array has been developed in collaboration with Prof. Susan E. Shore (at the University of Michigan's Kresge Hearing Research Institute (KHRI) and Sensory Neurobiology Laboratory) and her laboratory group, in particular Dr. Susanne Dehmel and Mr. Seth D. Koehler. The array is an application-specific design which targets the mapping of neural connections between the ventral cochlear nucleus (VCN) and dorsal cochlear nucleus (DCN) in guinea pig using up to 160 electrode sites and which can be used as a prototype for a central auditory prosthesis [117]. This device represents the first high-density, three-dimensional, mapping array for use in the guinea pig VCN-DCN. This chapter presents the array specifications, fabrication methodology, and assembly techniques for the first-generation two-probe array and for the full five-probe 160-site device.

## 6.1 Application-Specific Array Design

Array design was initiated by considering the significant geometrical constraints presented by the application. The design specifications then led to the selected three-dimensional structure. Subsequently, suitable two-dimensional probes were developed for the two CN regions, and the 3-D structure and mounting platform dimensions were finalized.

### 6.1.1 Anatomical and Surgical Constraints

The cochlear nucleus is located in the auditory brainstem. The operative procedure involves removing part of the skull and aspirating a small portion of the cerebellum to reach the DCN. The access hole is made as small as possible to avoid excessive bleeding and trauma, which could cause interference in the experiment or even the death of the subject. While the surgery directly exposes the surface of the DCN, the VCN is located farther ventral, lateral, and rostral, in particular if the anterior ventral cochlear nucleus (AVCN) is the targeted subdivision of the VCN. The surface of this region is not exposed in order to safeguard the stability of the subject. Fig. 6.1 illustrates the surgical opening.

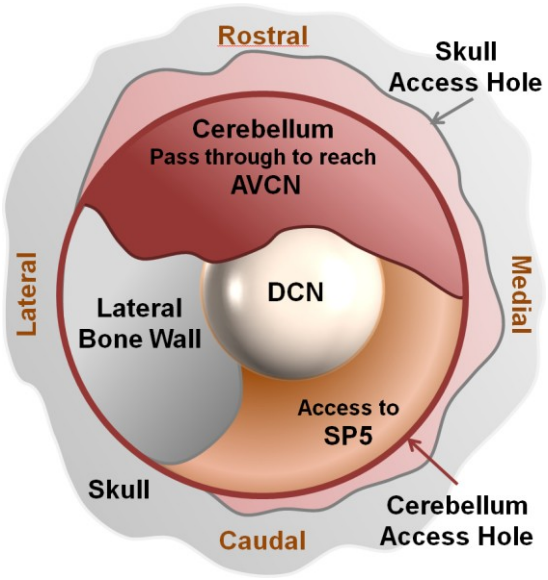



Fig. 6.1: Dorsal sketch of the surgical area; the cerebellum hole diameter is ~4mm.

The array must be inserted through the access hole in the cerebellum at an angle to reach the AVCN. The small diameter of the access hole and the angle at which the array is inserted leads to considerable size and position constraints on the electrode array, particularly on the platform and any required cabling. The difference in the medio-lateral location of the two subdivisions necessitates an offset between the platform positions of the probes designated for the respective regions. The relative dorso-ventral and rostro-caudal positions of the CN subdivisions also necessitates the insertion angle and relative probe lengths. To add to the complexity, variation in the subjects due to age, size, or other causes may also affect the relative location of the target tissue.

When considering the relationship between the somatosensory system and the auditory system, particular experiments involve stimulation in the spinal trigeminal nucleus (SP5) while recording in the CN. To enable these studies, the array platform must also be narrow enough for a commercial stimulation probe to be inserted adjacent to the array in the same access hole. Such studies prompted the development of the mapping array presented in this work. Researchers had sought to stimulate in SP5 with a concentric bipolar metal electrode (FHC, Inc., Bowdoin, ME) while simultaneously recording in VCN and DCN with two separate planar silicon probes (NeuroNexus Technologies, Ann Arbor, MI). Attempts were unsuccessful due to the small working space; the packaging for the planar probes was too bulky to allow both to fit, although the company's smaller chronic packaging had been selected. While this company now also supplies 3-D arrays, the orientation of the selected two-dimensional probes for one of their arrays must be parallel without horizontal offset. The relative anatomical position of VCN and DCN, as discussed above, call for more extensive platform possibilities.

While the basic anatomical structure of the guinea pig brain is well-known, the numerical details required for a single three-dimensional array to simultaneously reach VCN and DCN were not readily available from current literature. In order to better understand the relative positions of these subdivisions with the CN, mock-up arrays were assembled by Mr. Brendan Casey and implanted by Dr. Susanne Dehmel with fluorescent Fluoro-Gold (FG) dye on the probe shanks; Fig. 6.2 shows a tissue section with FG. Histology and three-dimensional reconstructions of the images, performed by S. Dehmel, provided the necessary information for probe and platform specifications.

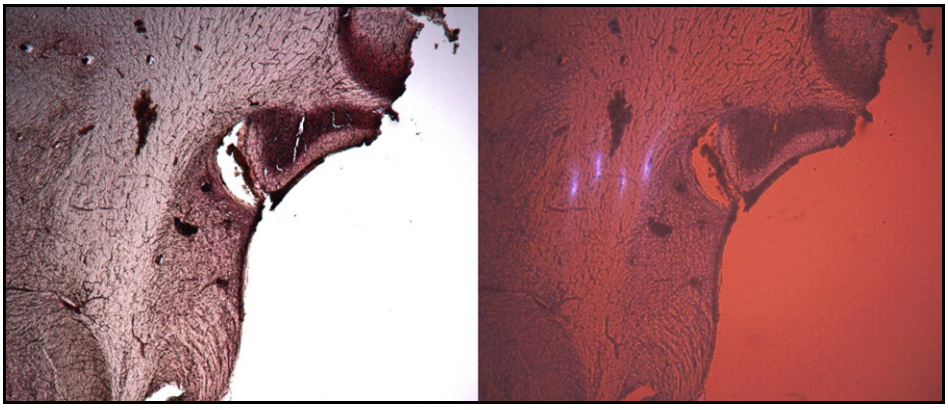


Fig. 6.2: Section of guinea pig right CN with neutral red stain (left) and same section under UV light (right) showing Fluoro-Gold tracks of the mockup array.

### 6.1.2 2-D VCN-DCN Probes for Use in the 3-D Array

In order to meet the design constraints, the VCN-DCN bidirectional neural interface array was designed to consist of five, 32-site, four-shank probes secured in a mounting platform to form the 160-site device. Two probe designs were developed, one for VCN and the other for DCN; specifications are listed in Table 6.1.

**Table 6.1: Specifications for Ventral and Dorsal Cochlear Nucleus Probes**

| **Probe Target Tissue** | **VCN** | **DCN** |
|---|---|---|
| **Probe Back-end Major Width** | 800μm | 800μm |
| **Probe Back-end Minor Width** | 661μm | 661μm |
| **Shanks per Probe** | 4 | 4 |
| **Shank Length (from platform bottom to center of tip-most site)** | 5000μm | 3400μm (longest shank) |
| **Shank Length Stagger** | 0μm | 125μm |
| **Shank Pitch** | 200μm | 125μm |
| **Maximum Shank Width** | 61μm | 61μm |
| **Minimum Shank Width** | 57μm | 31μm |
| **Tip to First Site Distance** | 103μm | 50μm |
| **Recording Sites per Shank** | 4 | 8 |
| **Recording Site Area** | $177\mu m^2$ | $177\mu m^2$ |
| **Recording Site Pitch** | 300μm | 100μm |
| **Stimulation Sites per Shank** | 4 | n/a |
| **Stimulation Site Area** | $1000\mu m^2$ | n/a |
| **Stimulation Site Pitch** | 300μm | n/a |
| **Integrated Cable Width** | 692μm (main) 742μm (across anchor) | 692μm (main) 742μm (across anchor) |
| **Integrated Cable Length** | 10mm | 10mm |

Three of the five probes in the array are targeted for VCN. The VCN probe design has a merged shank region, which extends beyond the bottom of the platform once assembled, and four shanks at a pitch of 200μm as shown in Fig. 6.3. The total length from the bottom of the platform to the center of the tip-most site is 5mm. The merged shank region remains outside of the cerebellum after implantation and spans the distance

to the platform required by the insertion angle and insertion depth. By merging this region the strength of the probe is increased and the impedance of the interconnect lines may be decreased, since their width may be increased.

Fig. 6.3: Layout of a 32-site, four shank probe for recording and stimulation in VCN. The transition to the integrated cable at the probe back-end is also shown.

Recording and stimulation offer conflicting constraints on electrode site area. Although single units may be more easily recorded with smaller sites, the amplitude of the possible or safe current would be less with the smaller-area higher-impedance sites. In order to both record and stimulate effectively with the VCN probe, and to do so at the same or nearly the same location, sites were arranged in pairs. The smaller site of each pair is designated for recording and has a site area of 177μm$^2$. The larger site of each pair is intended for stimulation with layout area of 1000μm$^2$. There are four site pairs per shank at a pitch of 300μm for a total of eight sites per shank and thirty-two sites per probe. The site designations of recording and stimulation are based purely on the site area. It should be noted that, aside from the above discussion, any of the sites are suitable for recording or stimulation.

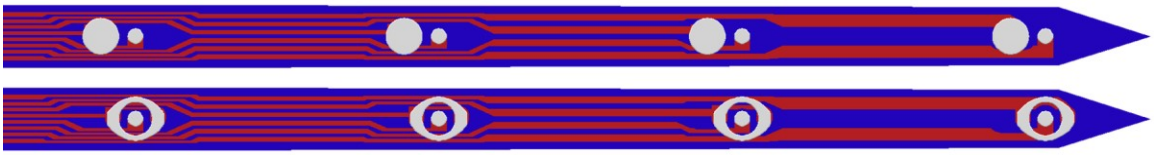


Fig. 6.4: Drawings of two VCN probe site configurations with adjacent (top) and concentric (bottom) arrangement for recording and stimulation.

There are two options for the VCN electrode site pairs as illustrated in Fig. 6.4. The first option is a standard linear configuration in which the recording and stimulation sites are placed adjacent to each other. The second option features a concentric site arrangement; the stimulation site encircles the recoding site. This novel layout was employed so that the region most affected by the stimulation current would coincide with

the region from which recording occurred, while also providing a smaller recording site area and larger stimulation site area. Examination of the utility of the concentric site pairs necessitates *in vivo* testing; this is enabled by an additional probe design, shown in Fig. 6.5 and Fig. 6.6, in which sites of both styles are closely spaced.

Fig. 6.5: Site comparison probe layout.

Fig. 6.6: Site arrangement of the of the site comparison probe.

The remaining two probes of the 3-D array are designated for the DCN. The DCN probe design has four shanks at a pitch of 125µm with staggered lengths as illustrated in Fig. 6.7. The desired recording location of the DCN is within the top layers, only up to a few hundred microns deep. Since the surface of the DCN is dome-shaped, the shanks were designed with staggered lengths to account for the surface curvature and maintain recordings within the top layers across a given medio-lateral probe position. The length of the lateral-most shank from the bottom of the platform to the center of the tip-most site is 3400µm; subsequent shanks each decrease in length by 125µm. There are eight equally spaced sites per shank as shown in Fig. 6.8 at a pitch of 100µm. All of the sites have an area of 177µm$^2$; although this site size is more favorable for recording, these sites may also be used for stimulation. Overlays of the probe layouts on histology slices were used during the design process to assist in determining the appropriate specifications; one such image is presented in Fig. 6.9.

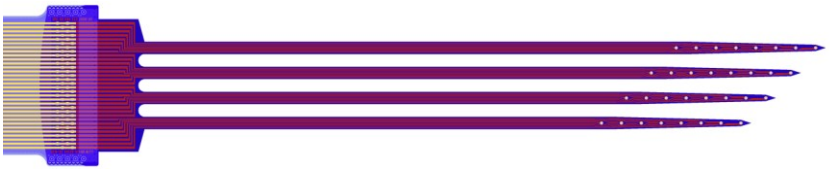


Fig. 6.7: Layout of a 32-site probe for DCN. A portion of the integrated cable is also shown. Note that the same scale is used in this image as in the 2-D VCN probe image in Fig. 6.3.

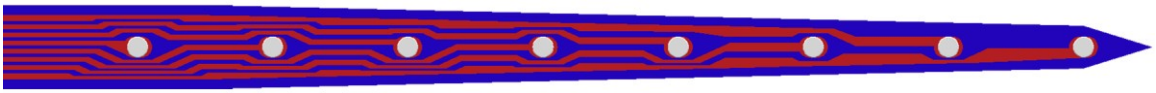


Fig. 6.8: Close-up of the DCN probe electrode sites layout.

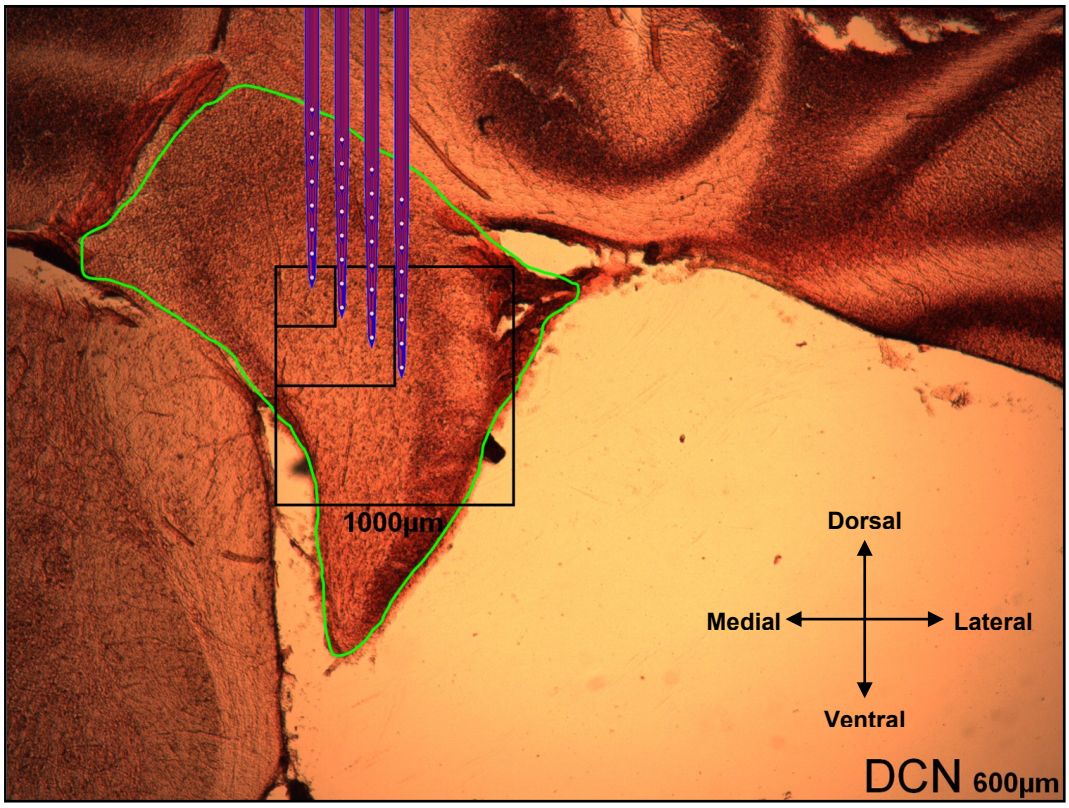



Fig. 6.9: Histology slice of the DCN from a 306g guinea pig with probe layout overlay. The overlay does not account for the angled insertion of the array. The histology, DCN outline, and scale bar were done by S. Dehmel.

Both probe designs had a maximum shank width of 61µm in order to minimize the disruption to the neural circuitry during implantation. This was achieved by using a minimum interconnect width of 2µm when necessary. The shanks also taper in the site region to keep the shank width at a minimum, as the interconnect lines reach their designated endpoints. Further details on the common aspects of the probe design and their integration into the three-dimensional array are given in the next section.

### 6.1.3 3-D Structure & Block Platform

Three-dimensional assembly has been done in the past by utilizing a thin platform through which two-dimensional probes are placed and secured with spacers. In this case,

the arrays may be regarded as multiple two-dimensional probes secured in parallel. The advances developed by Dr. Gayatri E. Perlin simplify the assembly process by constructing platforms from full thickness four inch silicon wafers and coutersinking the back-ends of the probes. This enables beam-lead bonding on the platform without obstructions caused by the probes themselves. A parylene overlay on top of the platform was used as the main layer of interconnect to carry the leads off the platform. This countersinking technique also eliminates the need for platform spacers to hold the probes parallel to each other. While this design significantly improves critical aspects of the assembly, it requires double bonding on the platform. Encapsulation requirements to prevent fluid from wicking up the probe shanks through the platform slots to the adjacent bonds should also be investigated before such a structure is used chronically and perhaps even acutely. Another design at the University of Michigan known as "Brain in the Box" took an alternative approach to alleviate platform bonding issues. This design incorporated two probes in a thin platform but utilized integrated cables on the probes so no platform bonding was required.

The present work combines the above two methods by using a block platform with countersunk probes and integrated cables. The VCN and DCN probes each include an integrated flexible cable 10mm in length as shown in Fig. 6.10. The cable is used to route the leads from the electrode sites on the silicon shanks, out of the surgical access hole, and to the next location. The cable terminates in an integrated silicon bond pad region with standard pad specifications. The pads are wire bonded to a rigid printed circuit board (PCB) probe stalk for the first-generation two-probe version of the 3-D array and to a commercial flexible PCB cable for subsequent mapping arrays. While integration of the cable adds to the processing complexity of the probe, it offers several advantages over the polymer overlay approach. The connection between the probe and the cable is formed during the fabrication process and thus does not need any post-process bonding. Ideally, the cable-silicon interface is also sealed due to secure attachment of the cable which prevents shorting by fluid leaking between the layers. An additional space-saving advantage of this methodology is that the cables may be "stacked" to form a "natural" multi-level interconnect. This is a significant feature for high-density designs such as the present work. The cable width is less than three-fourths

of a millimeter wide at its widest and carries thirty-two interconnect lines at 20μm pitch. The platform size constraints prevent expanding the platform to fit wider leads. In this context, the alternative approach is less attractive; to double bond this number of high-density beam-leads per probe to a platform and route them on a polymer overlay would not only require a wide polymer cable but would also increase assembly time and decrease yield.

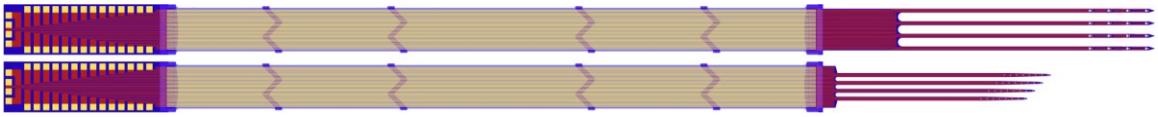


Fig. 6.10: Probe layouts with integrated cables and back-end bond pads.

The electrical and mechanical connections between the silicon probe and bond pad structures and the integrated cable are essential for proper functionality. Double contacts are made between the cable leads and polysilicon interconnects for increased reliability. A silicon anchor etch is employed to form mechanical "snaps," increasing the topology and thus the surface area contact between the silicon and cable. The anchor designs are based on previous work by Mrs. Mayurachat (Ning) Gulari. Silicon "zigzag" supports, developed by the work just mentioned, are also used along the cable to ensure the leads remain parallel.

The back-ends of the silicon VCN and DCN probes both employ the same design for countersinking into the platform. The platform is simply a slotted block of full wafer thickness (500μm) to mechanically secure the individual probes. A top, 300μm deep, and bottom, 200μm deep, etch form the probe slots and rim outline which releases the platform from the wafer. The top slot is wider than the bottom slot so that a ledge is formed upon which the probe rests when fully inserted as illustrated in Fig. 6.11. Between the major back-end width and the edge of the top slot etch there is a 15μm tolerance on each side. Even if the probe slides adjacent to one edge of the slot during assembly, the dimensions are such that the probe will remain on the ledge and then can be aligned before securing. The thickness of the slots is based on the target fabrication thicknesses of the layers; the next section includes a table of these values. The top portion of the probe back-end is designed to be 25μm thick. The top slots are 29μm thick for a 4μm tolerance. The bottom slot thickness extends past the top by 1μm on each side.

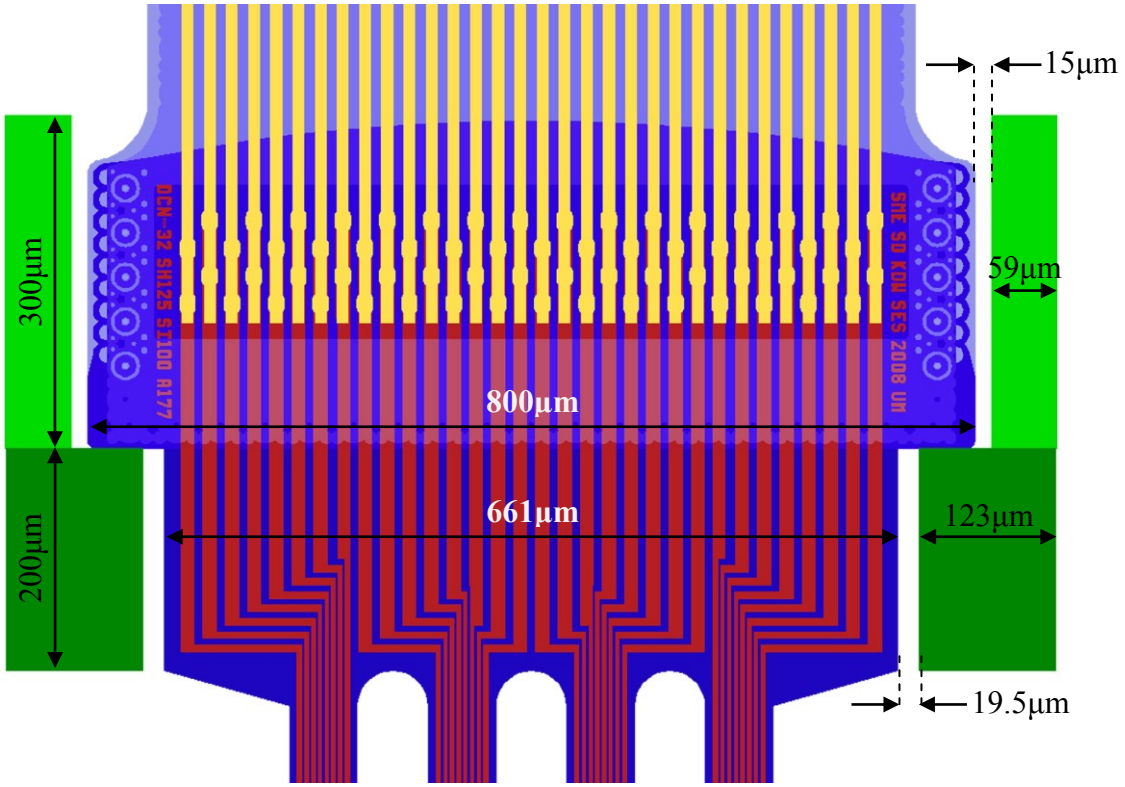



Fig. 6.11: Cross-sectional drawing of a 2-D probe in a platform slot. The light and dark green indicate the top and bottom slot etches of the full thickness wafer.

Several constraints led to the platform footprint for the VCN-DCN array. The viewing and placement region is extremely limited for surgical and experimental reasons as described above. Therefore, the medio-lateral and rostro-caudal dimension of the platform should be no larger than necessary to support the width of the probes. The narrow platform design supports probes with slots only 50µm from the edge of the platform in one direction and 59µm in the other. Since the VCN is more lateral than the DCN, the VCN probe slots are offset to the left of center in relation to the DCN slots. The VCN probe slot pitch is 300µm and the DCN probe slot pitch is 200µm. The distance between the closest DCN and VCN probe slots is 628µm. The VCN and DCN platform slots are perpendicular to each other in order to span the targeted subdivisions of the CN. The notched shape of the platform offers a reduced footprint over a rectangular shape design and allows greater visibility of the probe shanks during surgical implantation. The platform layout is presented in Fig. 6.12 and Table 6.2 lists the platform specifications. The 3-D 160-site array is illustrated conceptually in Fig. 6.13.

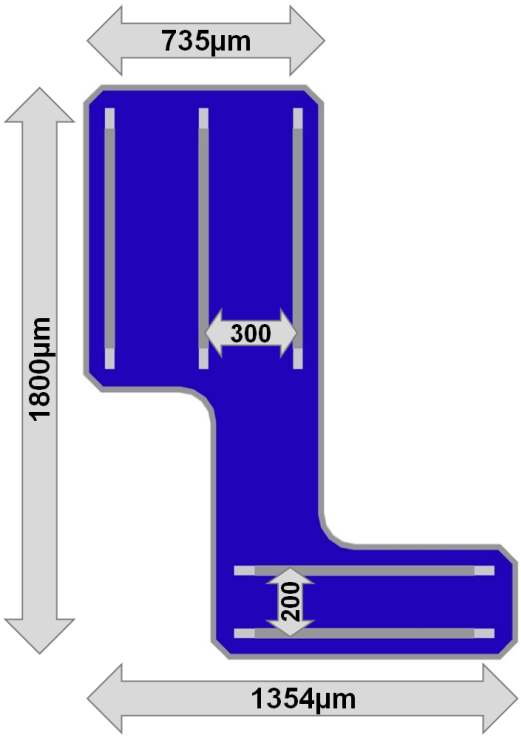



Fig. 6.12: Layout of the notched VCN-DCN block platform. Light gray indicates the top slot/rim etch and dark gray indicates the bottom slot/rim etch. Lateral is towards the left and rostral towards the top.

| Table 6.2: Platform Specifications for VCN-DCN 3-D Array | | |
|---|---|---|
| | **VCN Area** | **DCN Area** |
| **Length (rostro-caudal)** | 947µm | 335µm |
| **Width (medio-lateral)** | 735µm | 948µm |
| **Max Probes per Array** | 3 | 2 |
| **Probe Pitch** | 300µm | 200µm |
| | **Overall** | |
| **Total Length** | 1800µm | |
| **Total Width** | 1354µm | |
| **Thickness (dorso-ventral)** | 500µm | |
| | **Top (Major)** | **Bottom (Minor)** |
| **Slot Thickness** | 29µm | 31µm |
| **Slot Width** | 830µm | 700µm |
| **Slot Depth** | 300µm | 200µm |
| **Rim Etch** | 16µm | 17µm |

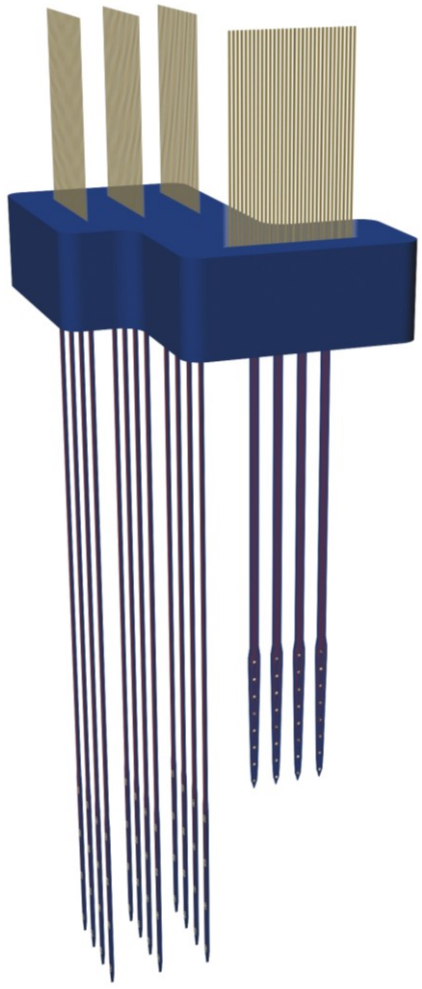


Fig. 6.13: A conceptual drawing of the VCN-DCN 3-D electrode array.

## 6.2 Probe and Platform Fabrication

The primary component required for a neural interface is the electrode array. The 2-D silicon probes in this work take advantage of the Michigan passive probe technology which employs boron etch-stops to enable thin (~12μm of silicon) devices to be batch fabricated with integrated polymer cables [68]. Table 6.3 delineates the major process steps and layer thicknesses for the 2-D probes. The block platforms were fabricated with deep reactive ion etching (DRIE) following a process similar to [59]. The fabrication of the MEMS devices and required process characterization was done at the University of Michigan Lurie Nanofabrication Facility (LNF) by Dr. Onnop Srivannavit and Mrs. Mayurachat (Ning) Gulari. Photos of released devices are shown in Fig. 6.14.

| Table 6.3: Probe Fabrication Steps and Target Parameters | | | | | |
|---|---|---|---|---|---|
| **Layer** | **Mask** | **Material** | **Etch** | **Thickness** | **Method** |
| 1 | BDF | Deep Boron | | 12µm | Diffusion |
| 2 | SHB | Shallow Boron | | | |
| | | Pad Oxide | | 1500Å | Thermal |
| | | Oxide | | 3000Å | LPCVD |
| | | Nitride | | 1500Å | LPCVD |
| | | Oxide | | 3000Å | LPCVD |
| 3 | POL | Doped Polysilicon Leads | x | 6000Å | LPCVD / Etch |
| | | Pad Oxide | | 1500Å | Thermal |
| | | Oxide | | 3000Å | LPCVD |
| | | Nitride | | 1500Å | LPCVD |
| 4 | LGCON | Large Contact | x | -- | RIE |
| | | Oxide | | 3000Å | LPCVD |
| 5 | SMCON | Small Contact | x | -- | RIE |
| 6 | IRD | Titanium (Ti) | | 500Å | Sputtered / Liftoff |
| | | Iridium (Ir) | | 3000Å | |
| 7 | GOL | Chromium (Cr) | | 500Å | Sputtered / Liftoff |
| | | Gold Pads (Au) | | 300Å | |
| 8 | DEL | Dielectric Etch | x | -- | RIE |
| 9 | XXX | Bottom Parylene | x | 2µm | Deposition / Etch |
| 10 | XP | Chromium (Cr) | | 250Å | Sputtered / Liftoff |
| | | Gold (Au) | | 1000Å | |
| 11 | AUP | Gold Beam (Au) | | 4-5µm | Plated / Liftoff |
| 13 | EXT | Silicon Anchor | 5µm | -- | DRIE |
| 14 | BSD | Top Parylene | x | 3µm | Deposition / Etch |
| | | Thinning | | | HNA or DRIE |
| | | Release | | | TMAH |
| | | | | | |
| | TOTAL | Back-end Top | | 24.875µm | All except 6 |
| | | Back-end Bottom | | 14.75µm | Through step 8 |
| | | Shanks | | 14.75µm | Through step 8 |

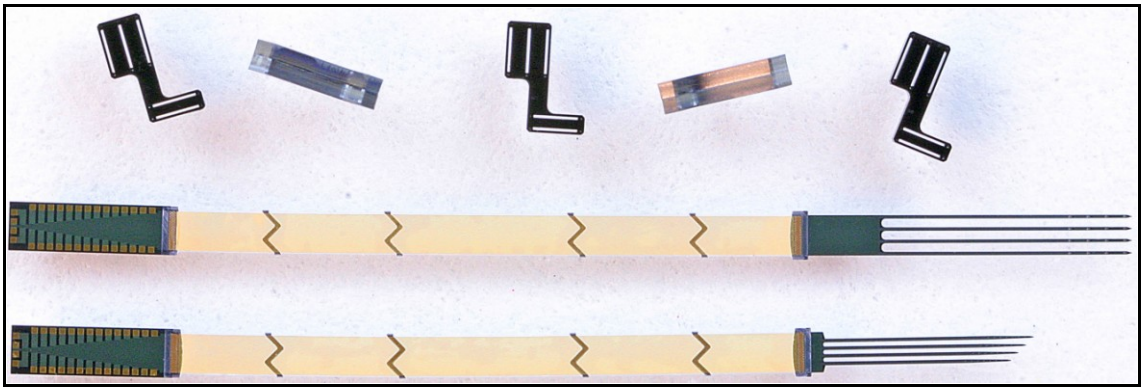


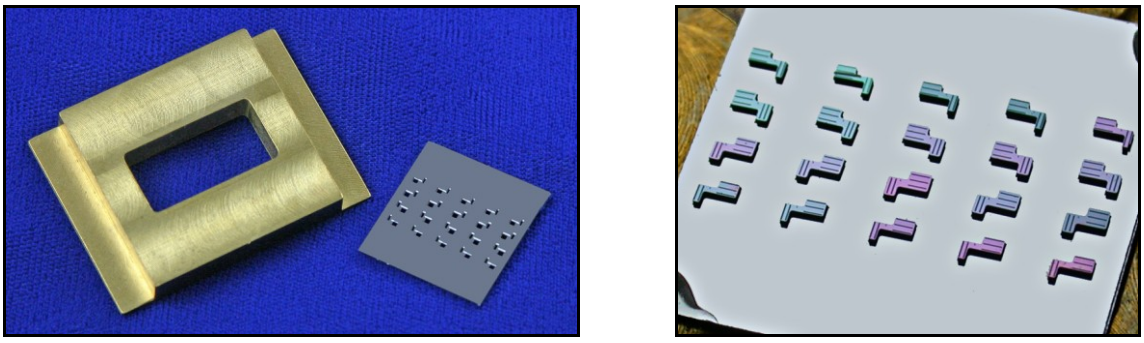
Fig. 6.14: Photograph of VCN and DCN probes and platforms.

## 6.3 Three-Dimensional Assembly & Packaging

Assembly and packaging are critical aspects of system integration for devices to be functional *in vivo*. This requires methods for handling and interconnecting the individual components. The following sections elaborate upon the assembly technique utilized to form the 3-D VCN-DCN array with 2-D probes and the packaging employed to handle the arrays for insertion and enable the leads to be connected to external recording and stimulation systems. Two packaging approaches were used, one for the first-generation two-probe device and the second for subsequent arrays including the 5-probe 160-site device.

### 6.3.1 Probe & Platform Assembly

The first step in the assembly process is the preparation of the appropriate equipment and tools with which to hold the platform and probes. The assembly station consists of a vacuum wand on a three-axis micromanipulator with base plate, a stereo-zoom microscope, and sufficient lighting as shown in Fig. 6.16. An assembly jig is used to hold the platform. This jig consists of a metal support block and silicon assembly holder in which recesses have been etched by DRIE for the platforms as displayed in Fig. 6.15. The holder is 500μm thick and the recesses are inset about halfway through the holder. The silicon assembly holder was machined with multiple platform recesses to enable assembly of several arrays at once. A span of tolerances between the platform dimensions and recess size was also tried; it is sufficient for the niche to be 5μm larger than the platform on all sides.



(a) (b)

Fig. 6.15: Photographs of (a) the metal support block, silicon assembly holder, and (b) VCN-DCN platforms loaded on the combined assembly jig.

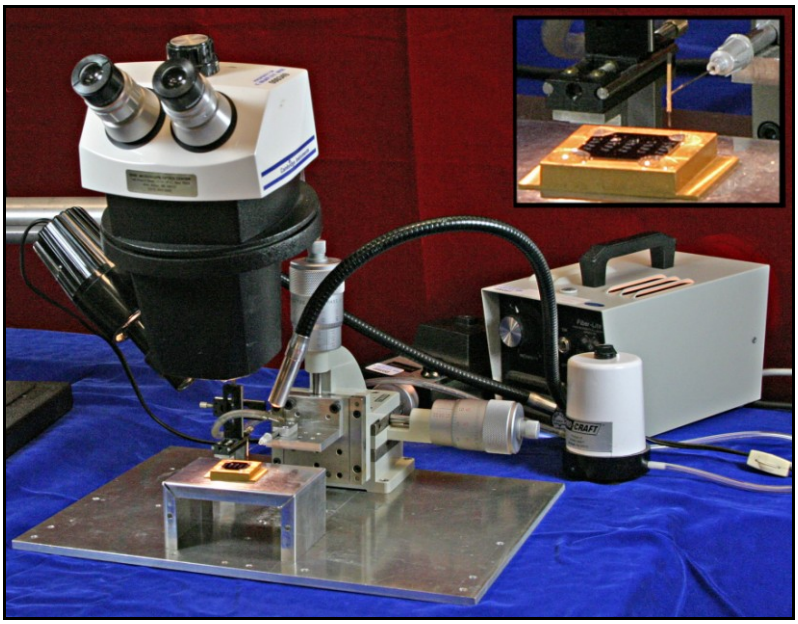


Fig. 6.16: Photograph of the assembly station. The inset shows a close-up of a probe on the vacuum wand and the assembly jig.

The platforms are placed with tweezers onto the platform holder and nudged into one of the intended recesses. If necessary, the platform can be prevented from moving within the niche by placing a small amount of dried liquid hand soap into the platform recess with a pulled glass pipette prior to inserting the platform. It was found that dried soap held with sufficient force but also made the array more easily removable than when the liquid form was used. A second vacuum wand is used to manually place a probe on the wand attached to the micromanipulator. The platform slot and probe are then aligned in the theta direction by moving the assembly jig and in the other directions with the micromanipulator. Once all of the probes are placed in the slots, a small amount of medical grade silicone (silastic) is used to secure them and to seal the top side of the platform slots. Care must be taken to ensure the silastic remains on the top of the platform. Surface tension acts in favor of this which makes the task readily manageable. The probes are straightened as necessary. After the silastic is cured, a slight nudge on the edges of the platform help to loosen it from the holder. Then the three-dimensional array is gently lifted out of the platform holder by grasping one of the cables with tweezers. If desired, the bottom opening of the platform slots can be sealed as well. The simplest method of handling the array for this task is to clamp one of the cables between two glass microscope slides. An assembled two-probe array is shown in Fig. 6.17.

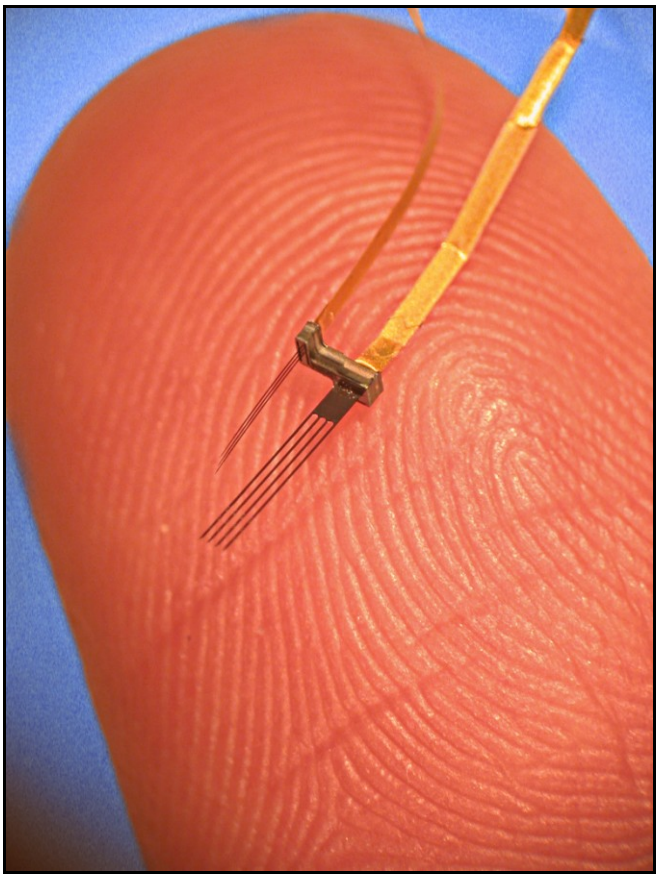


Fig. 6.17: Photograph of a first-generation two-probe VCN-DCN array on a fingertip.

### 6.3.2 First-Generation 2-Probe 64-Site 3-D Array

The initial version of the mapping array consists of two probes. This makes it possible to use printed circuit board (PCB) probe stalks to bring the leads from the cable ends to a commercial connector without the packaging becoming unfeasibly bulky. Although probe stalks are standard, the typical bonding methodology requires modification. Usually, a planar two-dimensional probe is attached to a probe stalk with an adhesive such as crystal-bond or epoxy which forms a solid base once cured. Then the probe stalk, with the attached probe, is placed on a glass slide and in a workholder for the wire bonder station, and normal wire-bonding is performed. The 2-D probe is flat, so there is little risk of damage to the device during bonding. The three-dimensional array provided additional challenges. One major complication is that the cables exit the array at different angles; when arranging the two cables to both come to parallel probe stalks this puts tension on the cables. The second issue with a 3-D device is that the delicate probes are exposed and raised from the flat surface of the glass slide subjecting them to

possible injury during bonding. In order to alleviate tension on the cables and to enable bonding without accidentally damaging the silicon front-ends or the cables, a custom workholder was created. The machining on the workholder was done by Sister Mary Joseph Campbell, O.P. It consists of a Plexiglas square about half an inch thick. Two slots are provided for the probe stalks with the connectors already soldered to them. The slots are at right angles to each other so the cables do not need to twist. After the connectors are in place, they are secured with Plexiglas straps to prevent accidental movement. The array platform and probes are gently inserted into a small hole in the top of the workholder so that the top of the platform is flush with the workholder surface. A small amount of epoxy is placed on the tip of each probe stalk and then the corresponding pad region of each cable is placed on the epoxy. Once the epoxy is cured, the pads are wire bonded to the probe stalk leads. Silastic is used to encapsulate the exposed conductor regions and as a stress relief at the transition from the integrated cable to the probe stalk. Fig. 6.18 shows the array-connector complex at this stage of packaging.

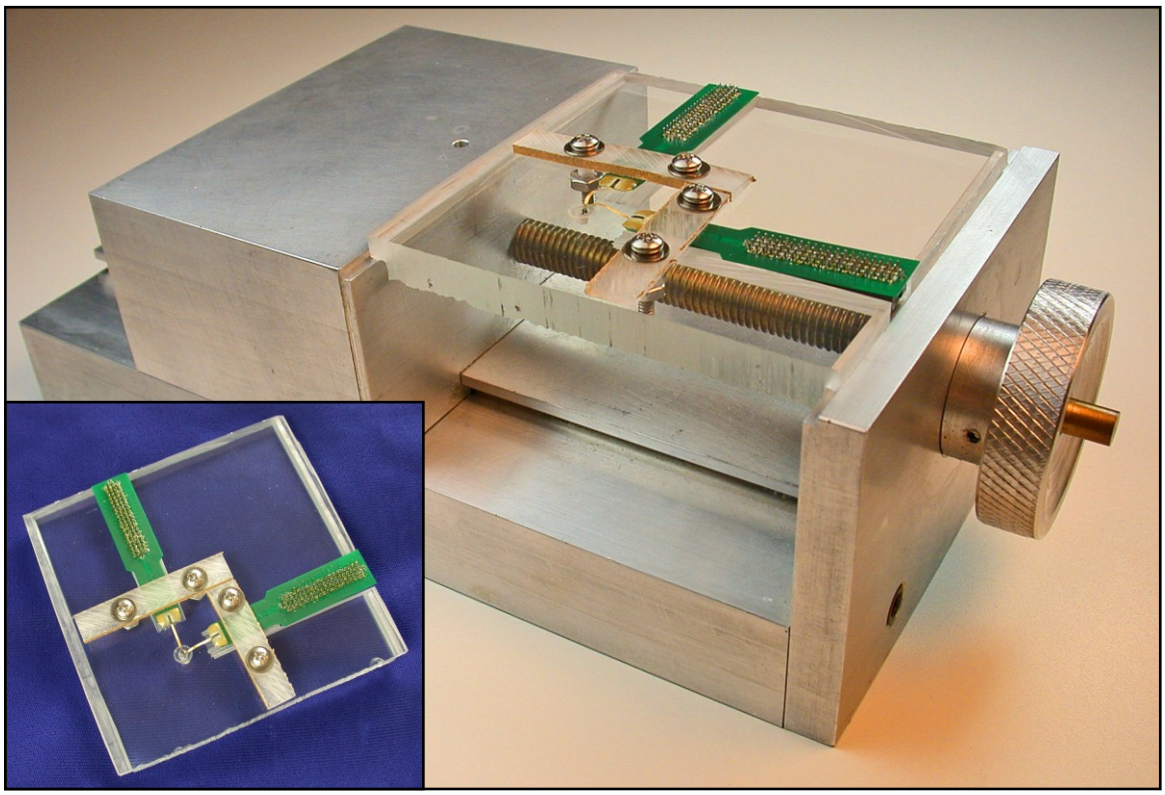


Fig. 6.18: Bonded array in the custom Plexiglas workholder (inset) with workholder in an aluminum clamp for stabilization during wire bonding and during the mounting of the tip of the insertion tool to the top of the array platform.

The next step is to secure the array to the insertion tool. The insertion tool consists of a dowel with a hollow metal tube attached at one end and a pin inserted in the tube and secured with epoxy. This tool is used to handle the array after assembly, in particular with the micromanipulator during implantation of the array during an *in vivo* experiment. To attach the array to the insertion tool, the tool is placed in a micromanipulator with a small amount of silastic or epoxy at the tip. The tip of the insertion tool is then aligned with the top of the array platform.

Once the array is secured to the insertion tool, it is raised with the micromanipulator out of the custom workholder hole. Then the two probe stalks are secured to the insertion tool to form one piece which can easily be manipulated by moving the insertion tool alone. A photograph of the completed first-generation two-probe array is presented in Fig. 6.19. Site connections for *in vitro* impedance testing, is straightforward; a ribbon cable is connected to the commercial connector on the PCB stalk and contact was made to the sites sequentially by contacting the appropriate locations on the other end of the cable.

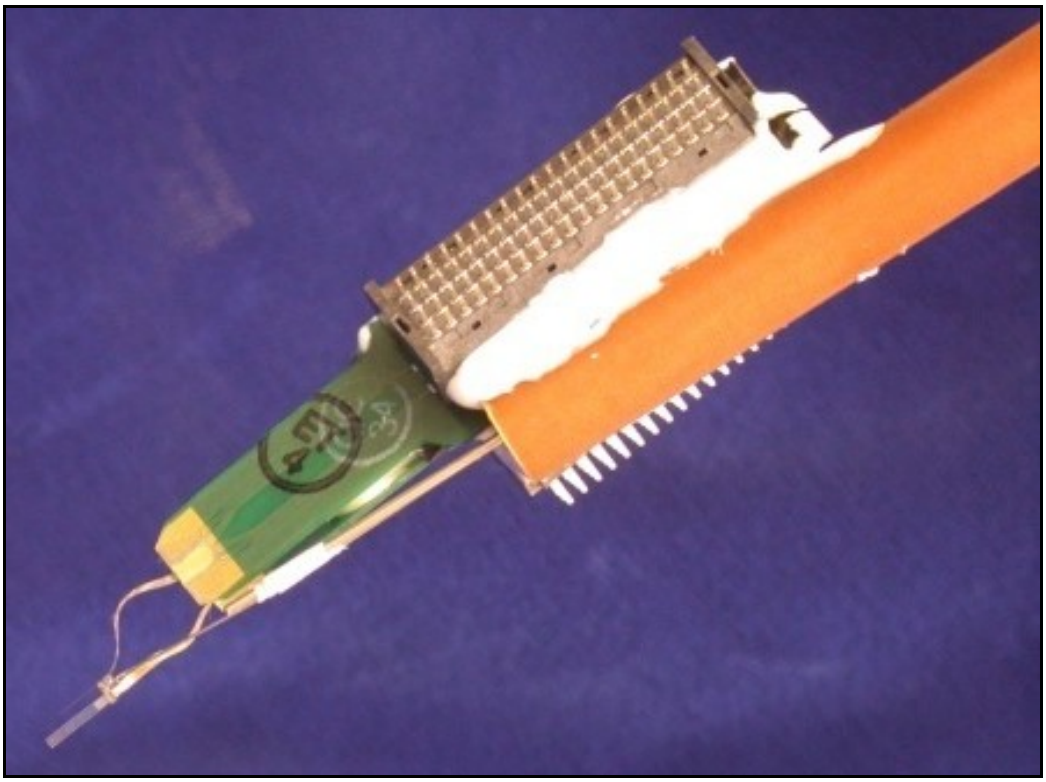


Fig. 6.19: Photograph of the first-generation array on the insertion tool with the two probe stalk connectors.

### 6.3.3 5-Probe 160-Site 3-D VCN-DCN Mapping Array

After initial *in vivo* studies verified the performance of the first-generation two-probe device, the final details were worked out to assemble and package the five-probe 160-site array which uses all of the platform slots. Several major challenges were overcome in moving from the two-probe to the five-probe structure. This included the connections and cabling from the integrated cables to the location of access to the leads on a macro level, the physical setup for assembly and bonding, and the final mounting to the insertion tool.

While the two-probe array makes use of standard printed circuit board (PCB) probe stalks to connect to the integrated polymer cables, it is not feasible to use five probe stalks since there is limited space to secure them, they would interfere with the surgical viewing, and the commercial ribbon cables that would then bring the leads from the probe stalk connectors to the site selection board would be impractically bulky. In order to overcome these difficulties a 25cm flexible polyimide PCB cable, shown in Fig. 6.20, was designed and manufactured (SunTech Circuits Inc.).

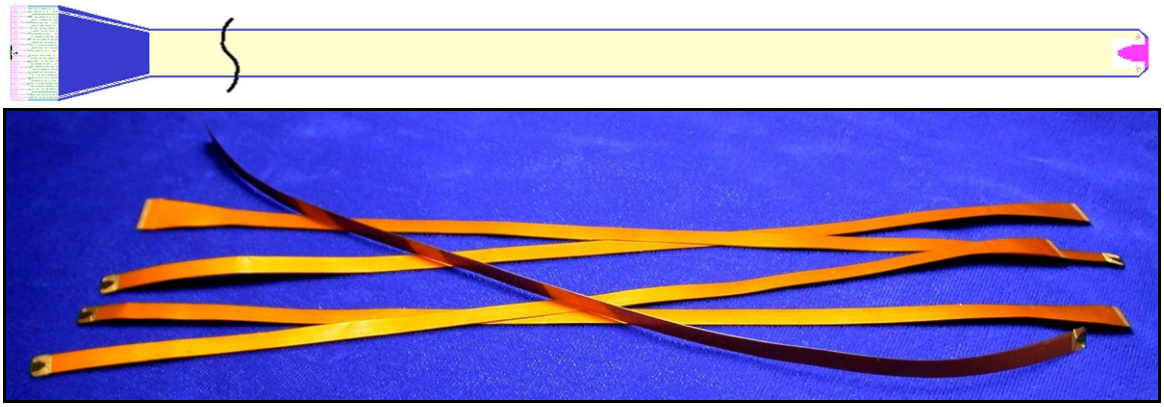


Fig. 6.20: Layout diagram (top) and photograph of flex PCB cables.

The second challenge was to devise a method for bonding the integrated polymer cables to the commercial flex cables. Initially probes were bonded first so they could be impedance tested and then inserted into the platform. Positioning a single probe attached to a cable in a slot was achieved multiple times but inserting a second in an adjacent slot was extremely difficult since it would be attracted to the first due to static. Therefore, a similar workholder was developed as used in the first generation to hold the assembled device and allow the cables to be bonded around it, as shown in Fig. 6.21.

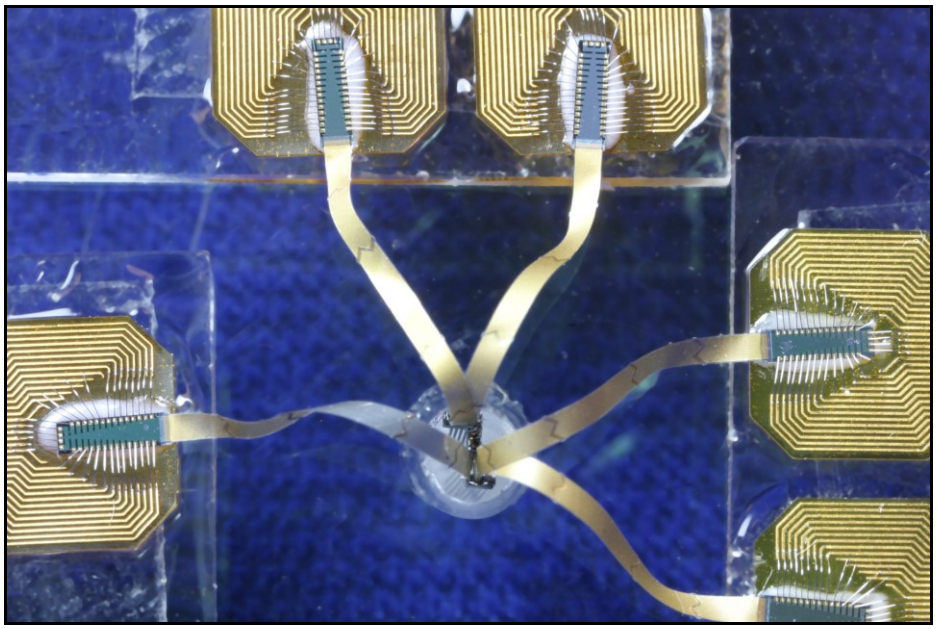


Fig. 6.21: Photograph of a five-probe array in the workholder machined by Sister Mary Joseph Campbell with the integrated cables bonded to the flex PCB cables.

The third phase of assembly and packaging is to connect the bonded array to the insertion tool. In order to better align the probe shanks with the insertion tool they were aligned and secured manually after removal from the workholder, as shown in Fig. 6.22. A photograph of a five-probe array is shown with a size reference in Fig. 6.23 and a close-up of the shanks is presented in Fig. 6.24.

Fig. 6.22: Photograph of a 5-probe array after attaching to the insertion tool.


Fig. 6.23: Photograph of assembled 160-Site VCN-DCN 3-D electrode array on the back of a U.S. dime.

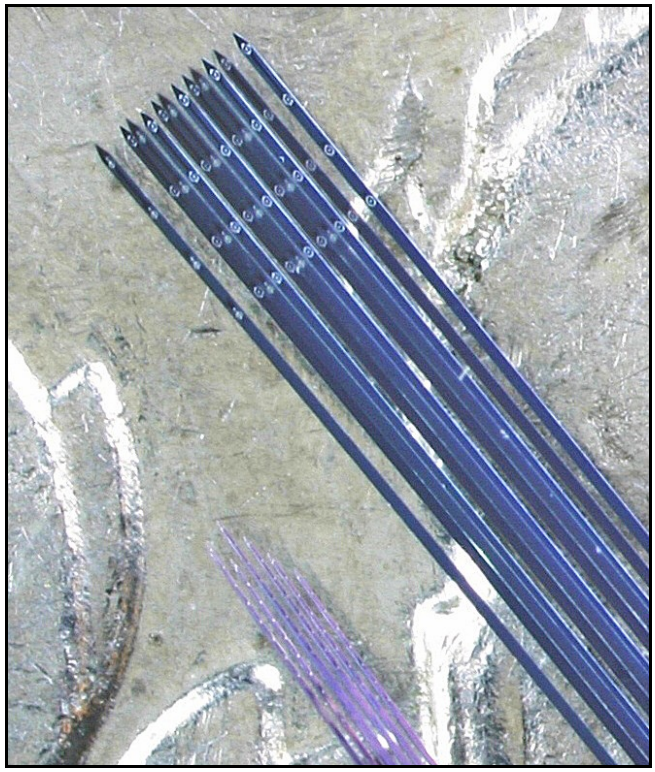


Fig. 6.24: Close-up photograph of VCN-DCN array shanks.

## 6.4 Conclusions

While high-density 3-D interfaces were made, challenges were encountered with the 2-D probes, the assembly process, attachment to the insertion tool, and *in vitro* testing, which future work should address. The parylene adhesion to the silicon was the least robust aspect of the 2-D probe design. Careful 3-D array handling techniques were necessary to avoid applying tension on these connections. It is surmised that main cause of unexpectedly high impedance (>3MΩ) on some channels was due to damage in the silicon-parylene connection. However, 177$\mu m^2$ sites with impedances over 8MΩ have still successfully recorded *in vivo*. Subsequent tests showed that increasing the parylene-silicon overlap area would enhance the adhesion. During the assembly process, while insertion of the probes into the slots was simple, aligning the probes once in the slots was more difficult than expected. The probes rotated in-plane and also angled out-of-plane. In order to improve probe-to-probe alignment, visual inspection and the tip of a pulled glass pipette was used to adjust the probes. Tighter platform tolerances would decrease the amount of deviation possible. Making the platforms thicker, for example starting with a 1mm thick wafer, would also assist in probe alignment and would not have any *in vivo* drawbacks in acute experiments. Another challenge was the alignment of the array with the insertion tool. This is necessary so that the array sharks are along the same axis as that of the micromanipulator movement to avoid slicing through the tissue during implantation. The most practical means of achieving this alignment might be to modify the insertion tool itself. Adding one or more joints to the tool would ease the alignment constraints at the array-tool interface as the joints could then be used to align the array-tool complex to the micromanipulator-axis. Impedance testing becomes more formidable as site number increases. While a LabVIEW interface was developed to assist in taking data, instrumentation which could automatically scan through all of the sites in an array would increase the practicality of the *in vitro* testing.

The presented device is the first 3-D array for mapping in the guinea pig VCN-DCN and represents one of the most advanced high-density neural interfaces ever reported. This application-specific device stands as a forerunner for future silicon-based electrode arrays which focus on target-specific neuroscience and medical needs, including neural mapping and prosthetic system prototypes.

# CHAPTER VII

# *IN VIVO* STUDIES WITH CONSECUTIVE AND CONCURRENT VENTERAL AND DORSAL COCHLEAR NUCLEUS RECORDING AND STIMULATION

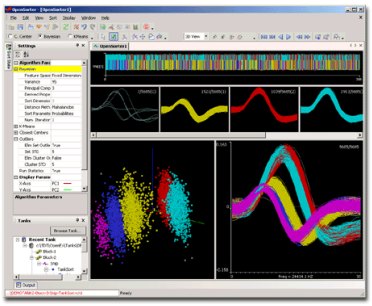
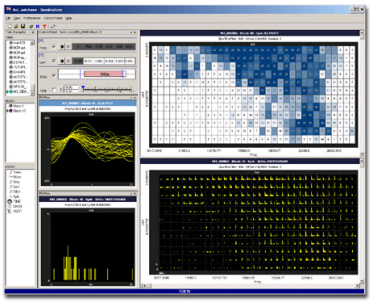
A concerted effort has been made in this research to place the 3-D array in the hands of neuroscientists where it will best be able to open new horizons of anatomical and physiological understanding. Towards this goal, multiple two-probe and five-probe devices have been assembled, packaged, impedance tested and then provided to Prof. Susan E. Shore's laboratory group, with whom this structure was developed. To date, seven *in vivo* experiments have been performed with the 3-D VCN-DCN arrays. The majority of the *in vivo* work, including the surgical preparation, probe implantation, experiment proper, and post-analysis, has been done by Dr. Susanne Dehmel. In order to delve more deeply into the biomedical application so to better meet the multi-disciplinary needs of the research, the author also participated in these experiments. The neuroscience focus of these studies has included frequency mapping, multi-region recordings, somatosensory integration, and mapping strategies with electrical stimulation.

This chapter presents the commercial equipment used for recording and stimulation, the site selection connector boards developed, and the surgical preparation. It also presents a selection of *in vivo* results gathered to date with these arrays when recording within a single CN subnucleus and recording simultaneously in both regions.

## 7.1 Commercial Recording and Stimulation Instrumentation

In order to create a versatile interface that is also tailored specifically to the instrumentation in the laboratory in which this *in vivo* work was performed, it is necessary to understand the available set-up and equipment. Table 7.1 lists the Tucker-Davis Technology components used in the experiments. The most critical part for integration with the array is the headstage. This sixteen channel input device has an eighteen-pin DIP socket header; the two topmost pins are reference and ground.

**Table 7.1: Commercial Instrumentation from Tucker-Davis Technologies**

| | Item (Part #) | Photograph/Details |
|---|---|---|
| **Multi-Channel Recording** | High Impedance Headstage (RA16AC) |  |
| | 16 Channel Acute Medusa PreAmp (RA16PA) |  |
| | Fiber Optic Link | |
| | Pentusa Base Station (RX5) |  |
| | OpenSorter & OpenExplorer<br><br>(Data Analysis) |   <br>OpenSorter is software for sorting neural spike data with methods including Bayesian expectation-maximization, k-means, and closest-centers algorithms. Data are displayed and can be sorted in principal components feature space, waveform parameter feature space, an event timeline, or piled waveform shape windows.<br>OpenExplorer is a data mining tool to explore the relationships between recorded data, stimulus parameters, and other events. |
| **Acoustic Stimulation** | OpenEx Software | |
| | Multi I/O Processor (RX8) |  |
| Information and images are from Tucker-Davis Technologies website www.tdt.com | | |

## 7.2 Connections Between the 3-D Array and Commercial Equipment

The specific packaging and lead transfers for the two versions of the 3-D electrode array, as presented in the previous chapter, enable access to the individual recording sites. This access is sufficient for impedance testing of the sites. However, not only are connectors, which correspond to the headstage inputs, required for *in vivo* recording, but it is also necessary to provide site selection capabilities since the number of available recording channels was limited to thirty-two at the time of the initial experiments. It is also desirable to plan for future system expansion for more recording channels. After considering the engineering advantages and disadvantages of passive and active site selection methods, it was decided to develop manual site selection connector boards rather than ones implemented with circuitry.

### 7.2.1 Manual Site Selection Board for the First-Generation 2-Probe Array

With sixty-four available electrode sites in the two-probe array, site selection is already an important factor. In preparation for *in vivo* experimentation, a connector board was essential so thirty-two of the sites could be selected for routing to the thirty-two inputs of the recording system. As infinite combinations can be unwieldy, the sites from each probe are split into four groups of eight. This enables selection of four site groups which may be on a single probe or from both probes. The recording sites of the DCN probe are arranged in groups by pairs of site "rows." This matches the anatomical/physiological arrangement of the neurons since the DCN is multi-layered in the dorso-ventral and medio-lateral directions. The VCN probe has sixteen sites designated for recording and another sixteen designated for stimulation; this forms a natural divide into two major groups. These groups each need to be divided in half to form groups of eight sites. In addition, the VCN probe is inserted at an angle in the caudal-rostral-ventral plane. Therefore, in order to match the physical site locations that might be best grouped together based on potential neurons from which they would record, the VCN recording sites are divided into an upper and lower triangle of sites. The VCN stimulation sites are similarly divided. Fig. 7.1 illustrates the site groups. A photo of the corresponding connection board is shown in Fig. 7.2. The selected sites groups are chosen with the four ribbon cables and the leads are routed to the headstage connectors.

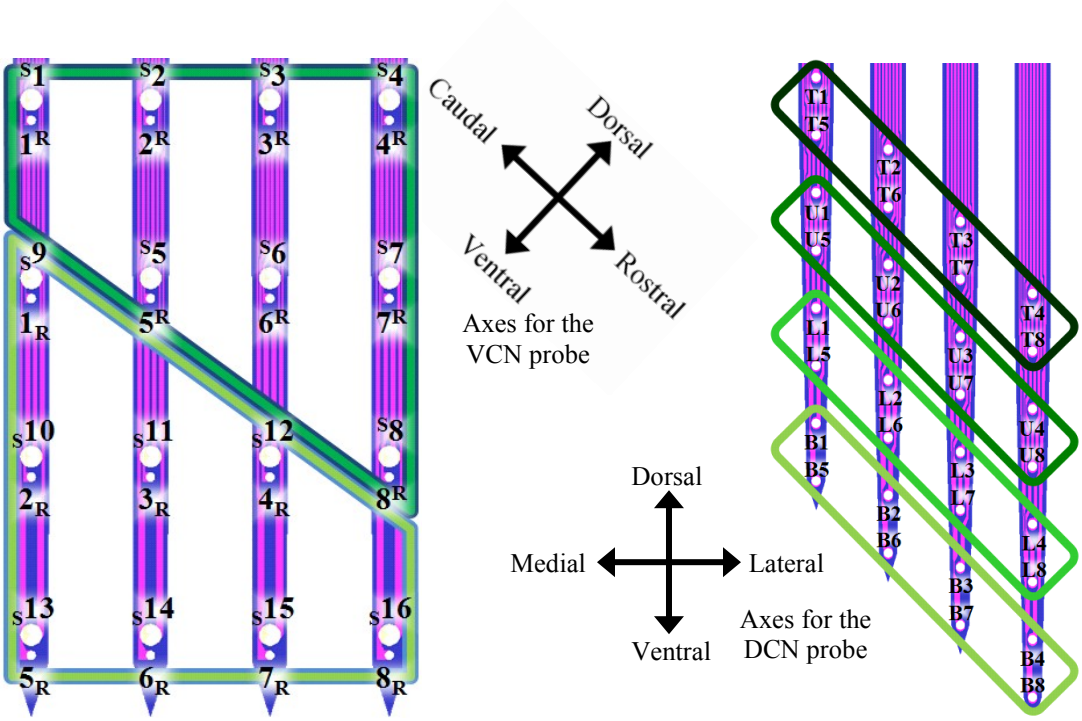



Fig. 7.1: VCN viewed from medial (left) and DCN viewed from rostral (right) site groupings for the 64-site connection board.

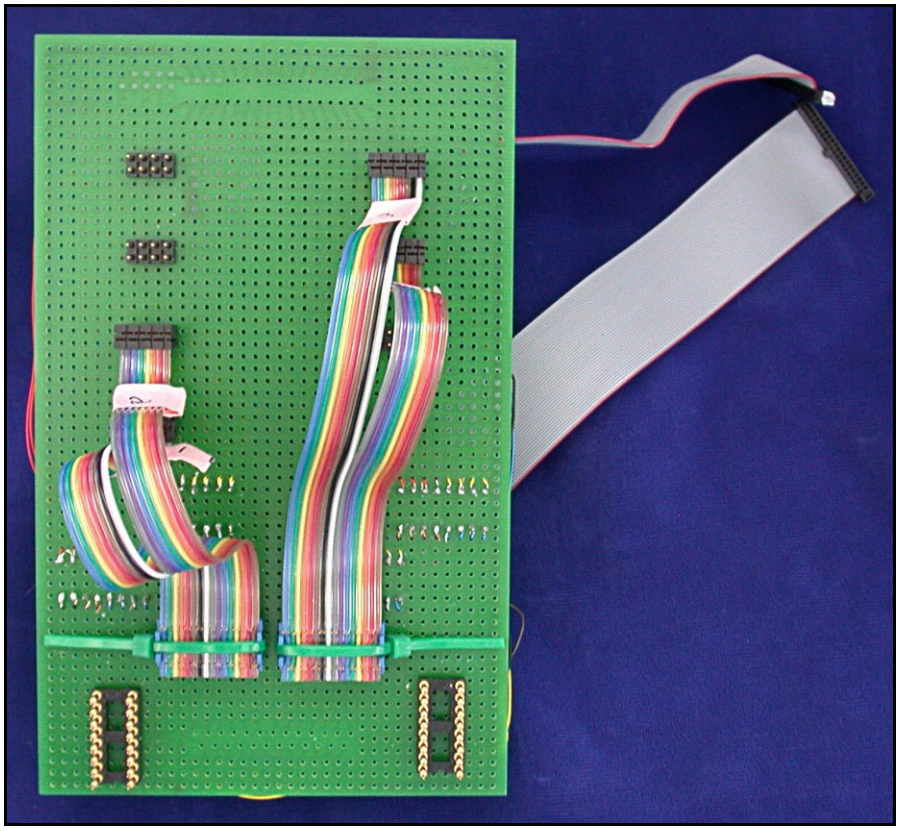


Fig. 7.2: Photograph of the 1st generation VCN-DCN connector board with 64-site input and 32-channel output.

### 7.2.2 Site Selection Board for the 5-Probe 160-Site Array

The five-probe array utilizes commercial flexible cables to bring the leads from the integrated polymer cables to the connection board as detailed in the previous chapter. Site selection is performed similarly as in the previous version. However, the site groupings were revised to make the real-time visualization of the signals during the experiments more intuitive. The recording software displays waveforms in multiple rows of four channels across. For the DCN probes, the rearrangement simply involved relabeling the sites across each "row" in the reverse numerical order since the neuroscientists preferred visualizing the probe from the caudal direction although the sites are actually located on the rostral side of the device. For the VCN probe, the sites were regrouped in rows similar to the DCN probe while maintaining the upper and lower designations and the separate groups for recording and stimulation site sizes. This change in part was due to the frequency mapping results from experiments with the two-probe device and also to make the VCN and DCN groups more consistent.

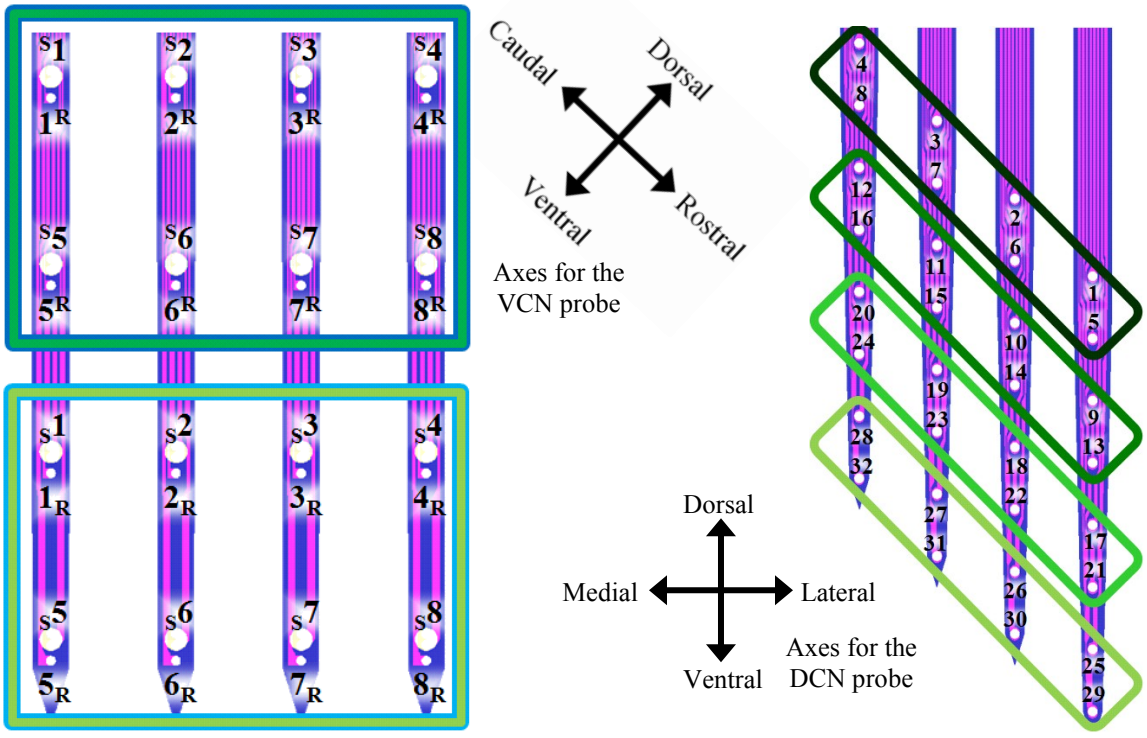



Fig. 7.3: Stimulation (blue) and recording (green) site groupings for the VCN probe (left), viewed from medial, and DCN probe (right), viewed from rostral, of the 160-site connection board. The VCN groups are named: stimulation top, recording top, stimulation bottom, and recording bottom. The DCN recording groups are: top, upper middle, lower middle, and bottom.

A photograph of the site selection board for the 160-site array is shown in Fig. 7.4, and Fig. 7.5 shows an example of each type of cable used in conjunction with this board. With 160 inputs, the routing was complex enough to warrant the fabrication of a custom PCB (through Advanced Circuits). The commercial flexible PCB cables, which bring the leads from the integrated cables of the 3-D array to the board, plug into the small surface mount connectors (HIROSE, FH35-33S-0.3SHW(50)) shown along the top of the board. These are labeled for identification of each from left to right: VCN lateral, VCN central, VCN medial, DCN rostral, and DCN caudal. The four site group connectors (square post header, Samtec, TSW-104-08-F-D) are located directly beneath the input connector for the corresponding probe. The VCN groups are: stimulation top, recording top, stimulation bottom, and recording bottom. The DCN recording groups are: top, upper middle, lower middle, and bottom. The 16-lead gray ribbon cable has a two by eight socket connector (IDC Assembly receptacle, FCI, 71600-016LF) on one end; the cable splits into two 8-lead ribbons which each terminate in a two by four socket connector (IDC Assembly receptacle, FCI, 71600-308LF). This cable, or one of similar design, is used to select two groups of eight sites and route them to one of the 16 pin connectors (square post header, Samtec, TSW-108-08-F-D) which in turn are routed on the PCB to the headstage connectors (screw machine dip adaptor, Samtec, APA-316-G-N). To ease external cabling constraints, the red jumper is used to short the ground line (G-Jump) from the input pins (A-Gnd) to the headstage ground pins (H-Gnd).

In order to support future expansion of the commercial equipment used in conjunction with this array or for setups in other laboratories, the board supports four sixteen-channel headstages for up to 64-channel outputs. This can easily be expanded to 128-channels by using the cables and headstage connectors of a second board in addition to the primary one. While site selection by groups is the most straightforward approach, at times a research protocol may desire more flexibility. As a means to facilitate this adaptability, the multi-colored cable allows for group independent site selection.

The single wire enables routing of the electrical stimulation from the input (C-Stim) to any selected site. The current stimulation can also be routed to multiple sites in parallel by connecting the selected site groups or individual sites with cables to the 16-pin connectors on the left third of the board which are shorted together for this purpose.

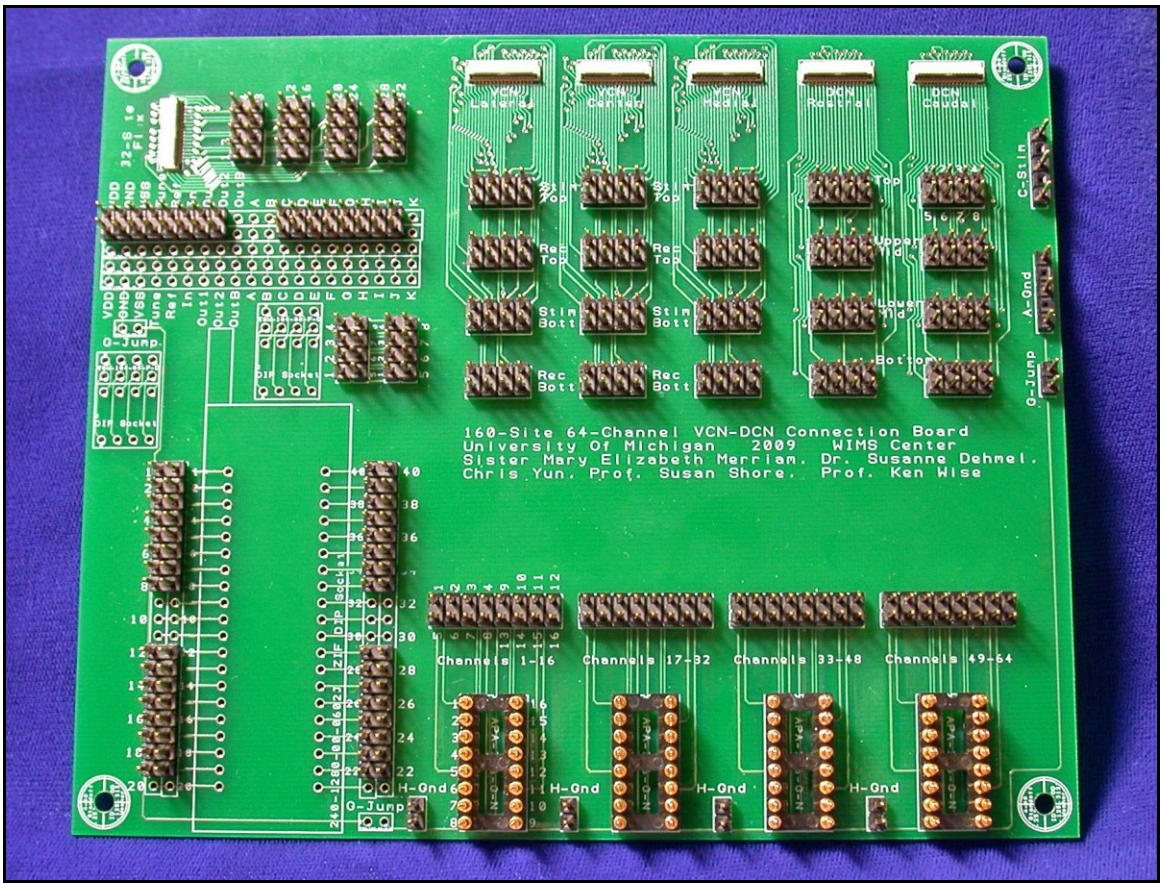



Fig. 7.4: Photograph of the 160-site input, 64-channel output connector board. This board is designed for up to four 16-channel headstages. The setup can be expanded to 128-channels by using two connector boards.

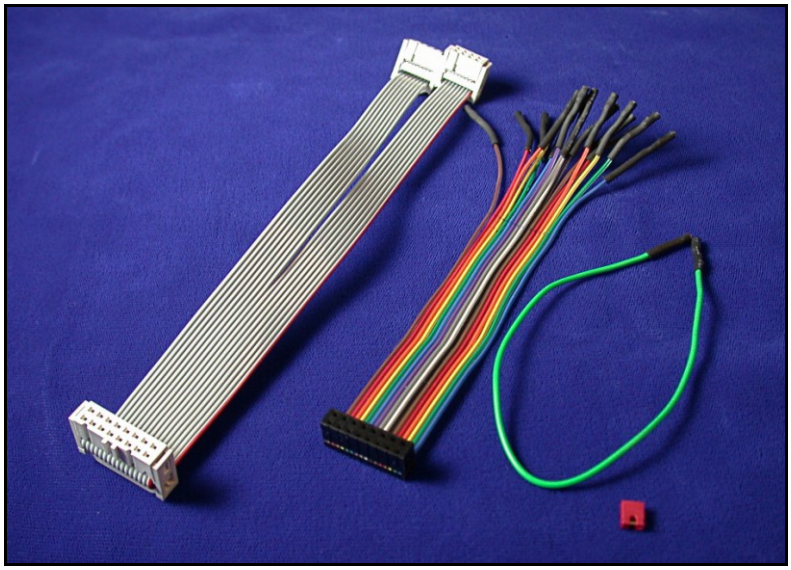


Fig. 7.5: Photograph of an example of each type of cable/component for use with the 160-site input, 64-channel output connector board for group or group-independent site selection as well as for the electrical stimulation routing.

### 7.3 Surgical Approach and Anatomical Location

The typical surgical preparation of the recording and stimulation experiments was as follows. Pigmented guinea pigs (Elmhill Farms) of young adult size/age (300-800g) were used in these studies; the animals were anesthetized using Ketamine (40mg/kg) and Xylazine (10mg/kg). A stereotactic frame, as shown in Fig. 7.6, stabilized the subject during surgery and recording which took place in a double-walled sound booth. The surgery included a craniotomy and partial aspiration of the cerebellum over the DCN, as illustrated in Fig. 7.7. Hollow earbars joined to speakers (Beyer DT770pro) provided the acoustic stimulus.

Fig. 7.6: Photograph of the equipment setup in the double-walled recording booth.

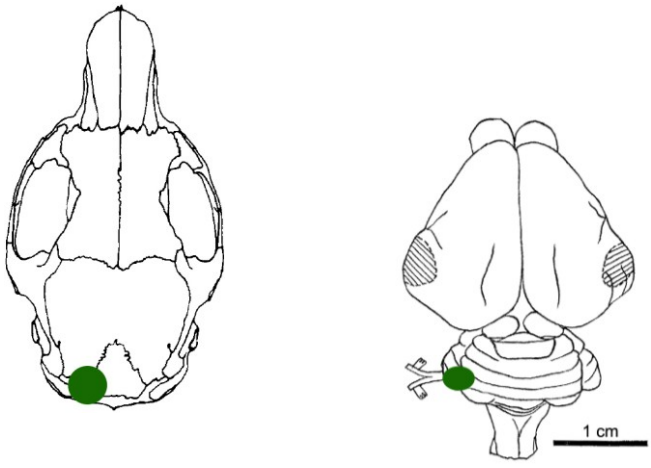



Fig. 7.7: Modified sketches of a guinea pig skull [118] and brain [119] to show surgical location.

The VCN-DCN 3-D array was implanted stereotactically through the access hole in the cerebellum as shown in Fig. 7.8. Direct visualization of the DCN surface was enabled by the surgical preparation. In order to reach the AVCN subdivision, the array was inserted at an angle; in other words, the platform surface was not parallel with the dorsal-most DCN surface. The animal ground was defined by connecting the neck muscles to the ground and reference pins of the headstage. During the initial portion of the experiment, acoustic stimulation coupled with extracellular recording assisted in the final placement of the array.

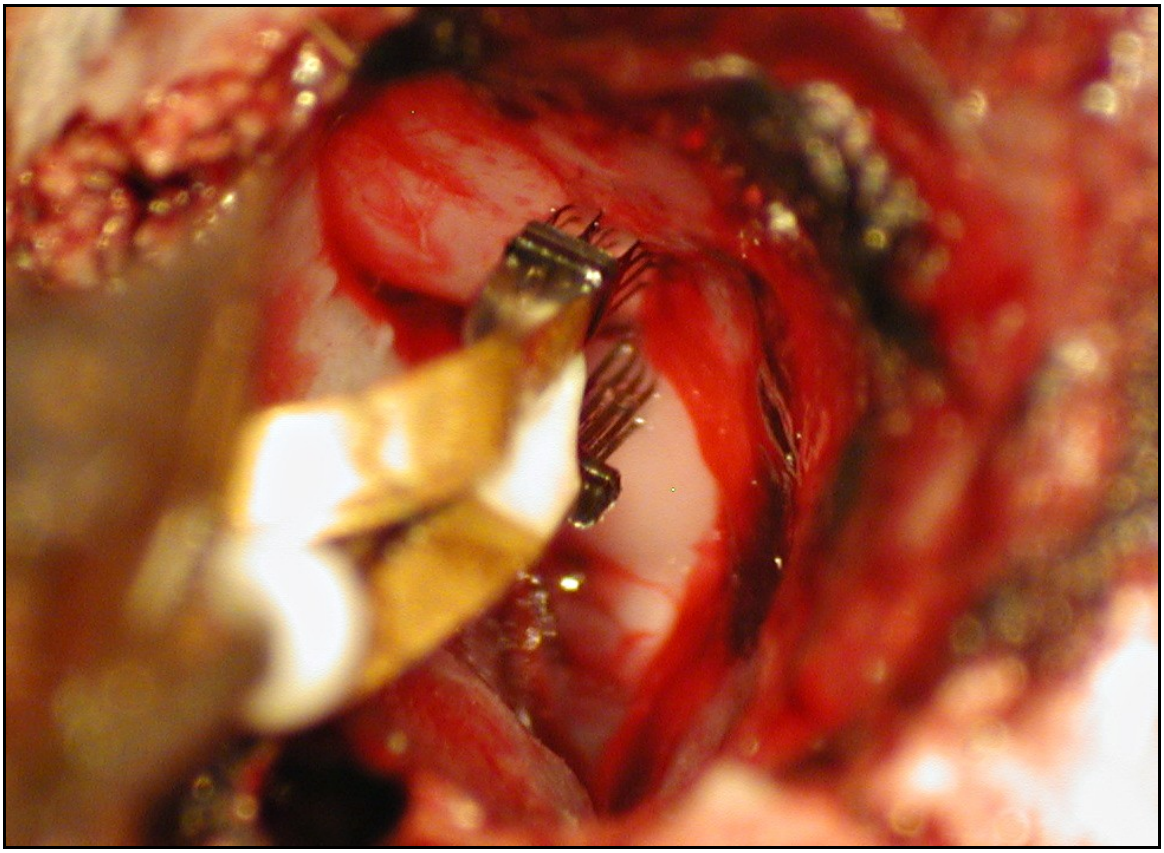


Fig. 7.8: Five-probe array implanted in the CN of a guinea pig. Photo by S. Dehmel.

Anatomical understanding of the guinea pig brain assists not only in proper implantation of the array but also in performing the *in vivo* recording and stimulation and in the interpretation of the resulting data. Fig. 7.9 shows the position of the CN within the auditory brainstem with the domed surface of the DCN clearly visible; the AVCN is located farther rostral and lateral than the DCN as indicated in Fig. 7.10.

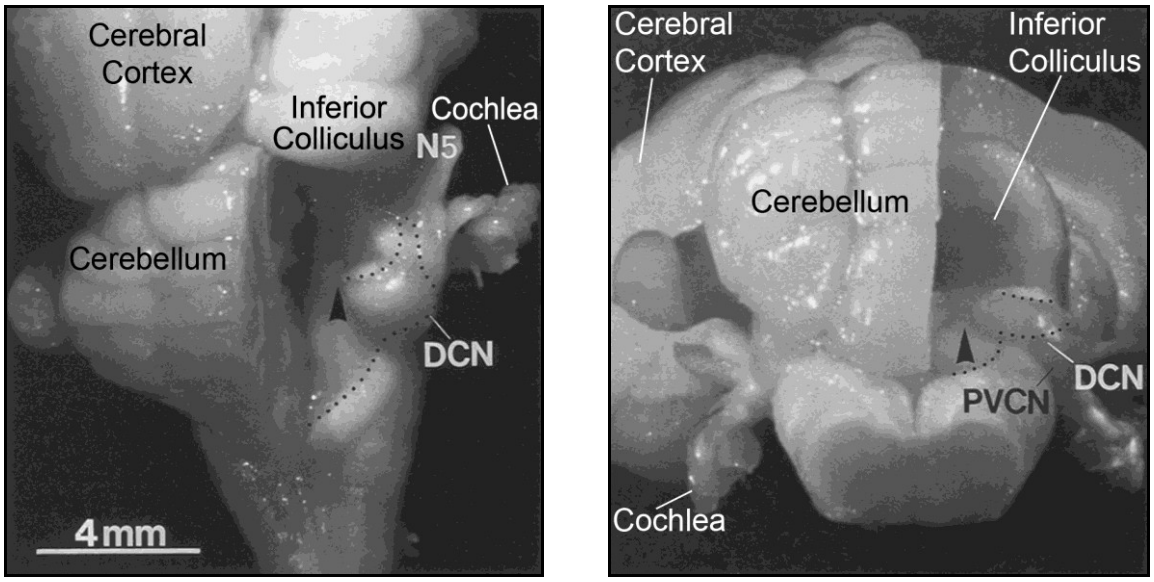



Fig. 7.9: Dorsal (left) and caudal (right) view photographs of a guinea pig brainstem after partial removal of the cerebellum and forebrain, both modified from [120]. The trigeminal nerve is labeled N5. The dotted line shows the taenia choroidea and contour of the cut cerebellar peduncles. Arrows point to the dorsomedial-most point of the DCN. Compare with Fig. 7.7.

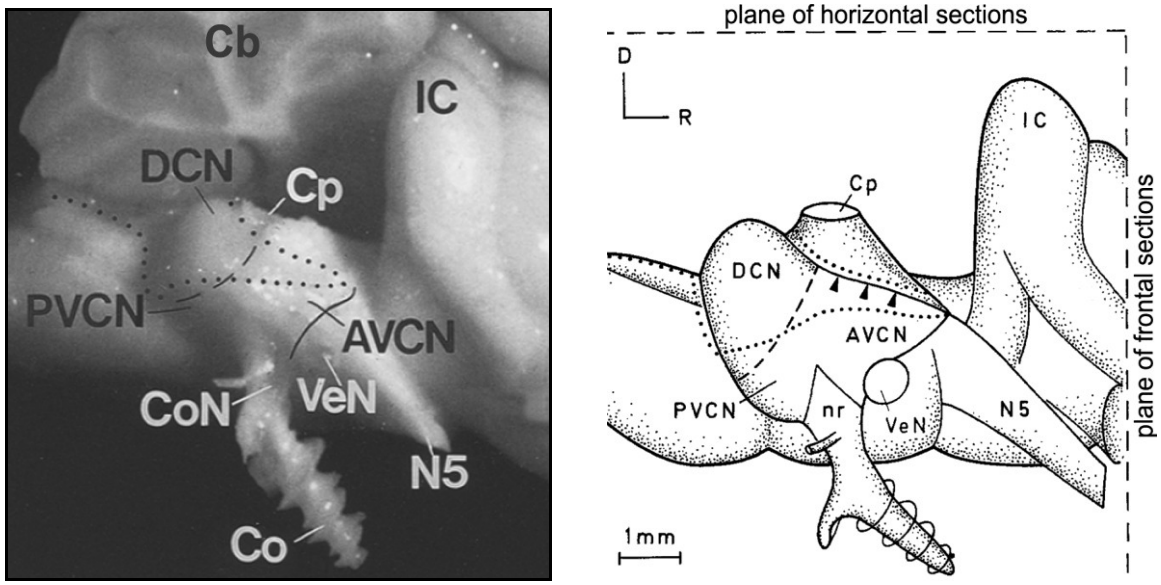



Fig. 7.10: Lateral view (animal's right side) photograph of a guinea pig brainstem (left) after partial removal of the cerebellum and forebrain and sketch of a similar view (right), both modified from [120]. Abbreviations are as follows: Cb, cerebellum; Co, cochlea; CoN, cochlear nerve; Cp, cerebellar peduncles; IC, inferior colliculus; N5, trigeminal nerve; nr, cochlear nerve root; VeN, vestibular nerve. The dashed and solid lines mark the rostral borders of the DCN and VCN respectively. The dotted line shows the taenia choroidea and contour of the cut cerebellar peduncles. In the sketch, the arrows indicated the dorsal edge of the VCN.

## 7.4 Single Unit Isolation

Extracellular recordings are of multiple types. Local field potentials (LFP) are slow wave oscillations, which represent the combined waveform of many neurons [121]. Multi-unit recordings are the responses of more than one neuron recorded through a single electrode site. Since much of the current neuroscience knowledge is based on single neurons, either isolated from or within the neural network, researchers typically seek waveforms of individual neurons. Advanced signal processing techniques can be used to extract the response of individual neurons from a multi-unit recording [122]. This can be aided by recording from the same or similar set of cells with multiple electrodes in close proximity (~20μm) to each other. Particular site configurations used for this include tetrodes. These post-processing strategies can even enable location identification of the neuron with respect to the array.

Another approach is to seek to record from distinct (sets of) neurons from each site, which simplifies the required post-processing during data analysis. To support this, it is advantageous to set the site spacing so that each site records from different neural populations. Cluster analysis is used to predict if a recording is due to a single unit, that is waveforms which are solely (or primarily) due to an individual neuron. Whether or not single unit isolation is achieved is due to a number of factors including electrode characteristics (geometry, material, impedance) and array placement (distance from site to closest neuron, type of neural tissue). Fig. 7.11 presents the cluster analysis and spike clips for one of the single units recorded during VCN-DCN array experiments; most recordings were multi-unit. Future work should improve single-unit recording methods.

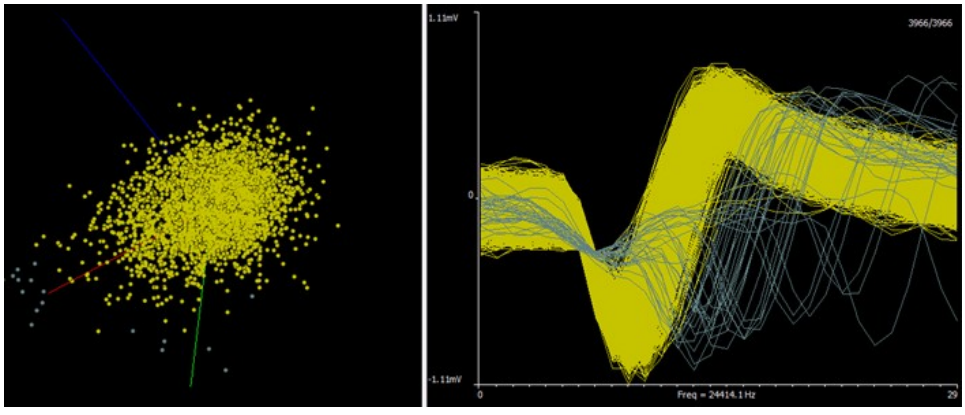



Fig. 7.11: Cluster analysis for single unit isolation (left) and corresponding neural waveforms showing overlaid spike clips of a single unit (right, yellow).

## 7.5 Intra-Region Recordings

Deepening the medical and scientific communities' understanding of the auditory system is an important step towards diagnosing conditions, selecting treatment, and developing further ways to address maladies, as well as towards forming a basis for further understanding other parts of the brain. As the first brain processing center, the cochlear nucleus plays a key role within the auditory system. This complex can be better comprehended both by learning about the details within its subdivisions as well as studying the connections between regions and the bidirectional signals between the CN and other anatomical centers.

### 7.5.1 Perspectives on Responses Characteristics

The complexity of the CN is underscored by its diverse cytoarchitecture. Fig. 7.12 diagrams over ten cell types, which are grouped in part by location, and shows the overarching tonotopic organization. Each cell type has particular response characteristics by which it can be identified using recording techniques and data analysis.

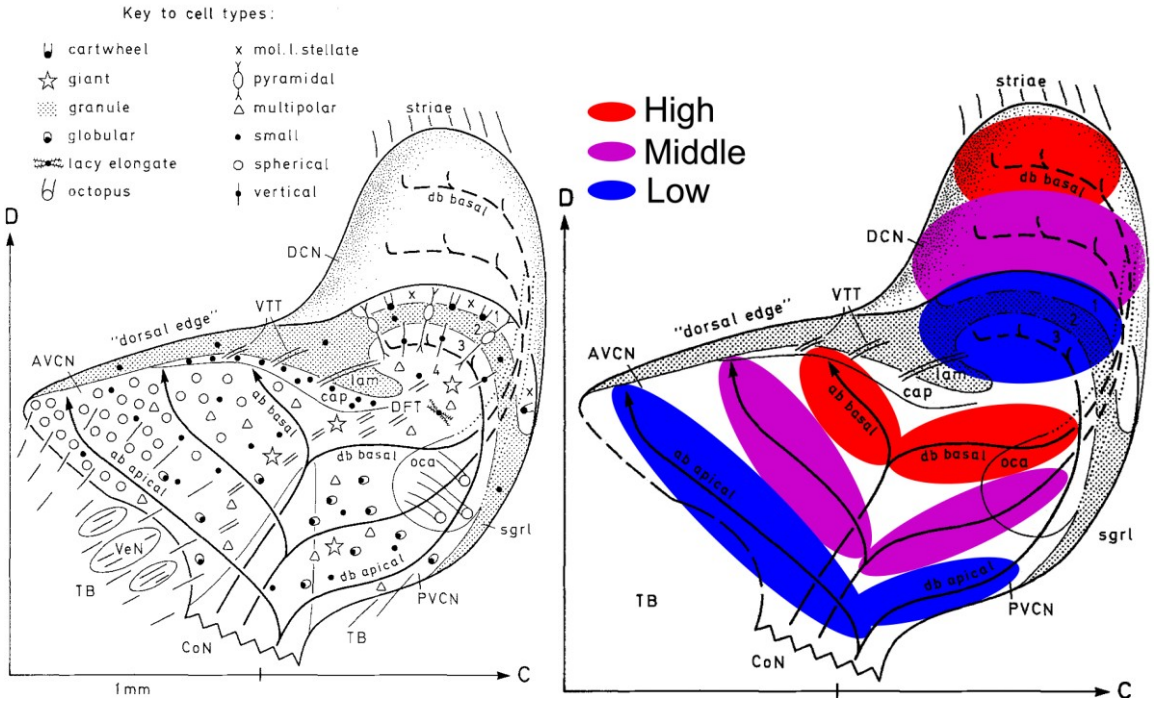



Fig. 7.12: Sagittal plane sketch of the guinea pig CN illustrating the main cell types and fiber tracts from [120] and modified with color overlays showing the tonotopic organization; see also [123].

When recording neural signals several things must be accounted for, including the background noise or field potentials and the typical firing rate without stimulus of a particular channel. Therefore, the stimulus is started some milliseconds into the recording time frame and ends before the end of the frame. A recording block includes the repetition of frames in order to obtain statistically relevant information on spike count during the stimulus in comparison to that before or after the stimulus. The neural responses are recorded as waveform voltage over time. Real-time signal processing software is used so that the signals and particular features can be observed during the study and so immediate decisions can be made during the experiment. First the thresholds of each channel are set, automatically or manually, in order to determine the voltage levels beyond which a signal will be counted as a neural spike. Once thresholding has been completed, spike clips are overlaid, spike rasters are charted, and histograms plotted. The post-stimulus time histogram (PSTH) is one of the main visualization tools for immediate verification of responses. The time frame is divided into small time bins; the per bin spike count of the repeated frames in a block summed and the total spikes per bin are plotted. Fig. 7.13 presents the PSTH recorded for one channel in response to an acoustic noise burst; the spikes per bin are significantly greater during the stimulus than either before or afterwards.

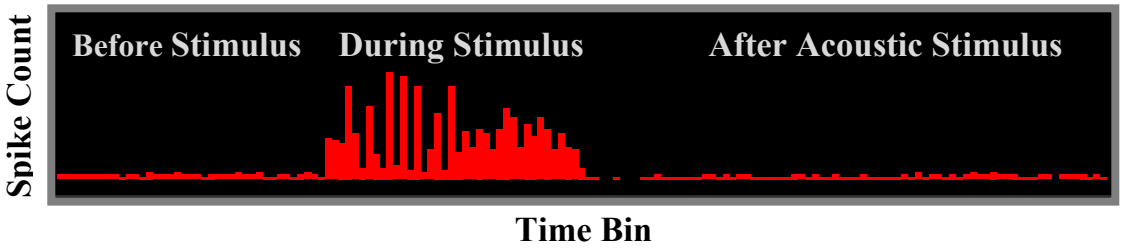



Fig. 7.13: Recorded PSTH of an elicited response due to a 70dB acoustic noise burst.

When stimulated with a tone at its characteristic frequency, the corresponding PSTH of a CN cell is one indicator of cell type. Fig. 7.14 shows sketches of the distinguishing shape of PSTHs for five main CN cell types from both subdivisions. A spread of patterns has been observed from recordings with the VCN-DCN arrays; a selection of these responses is presented in Fig. 7.15 for both subnuclei. In this work, typically characteristic PSTHs were recorded with 500 repetitions at a sound level 20dB above the threshold of the unit.

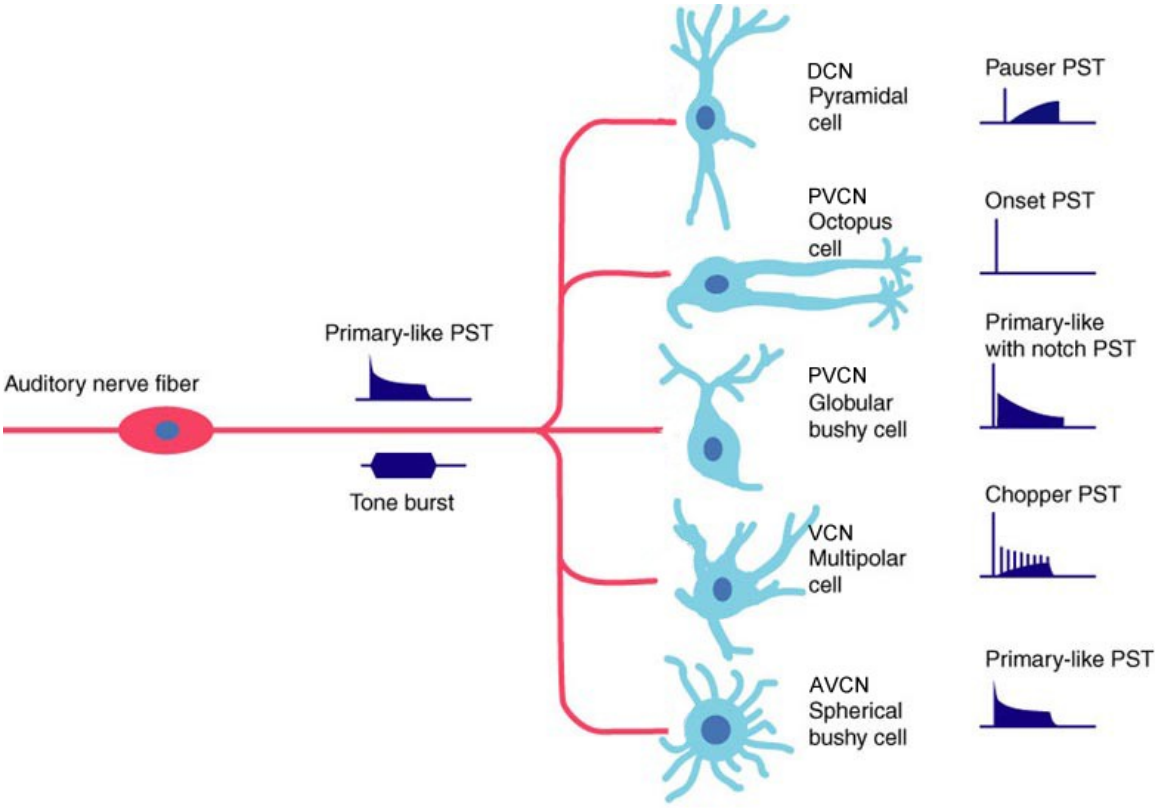





Fig. 7.14: Diagram of PSTHs corresponding to main CN subregion cell types, modified from [124].

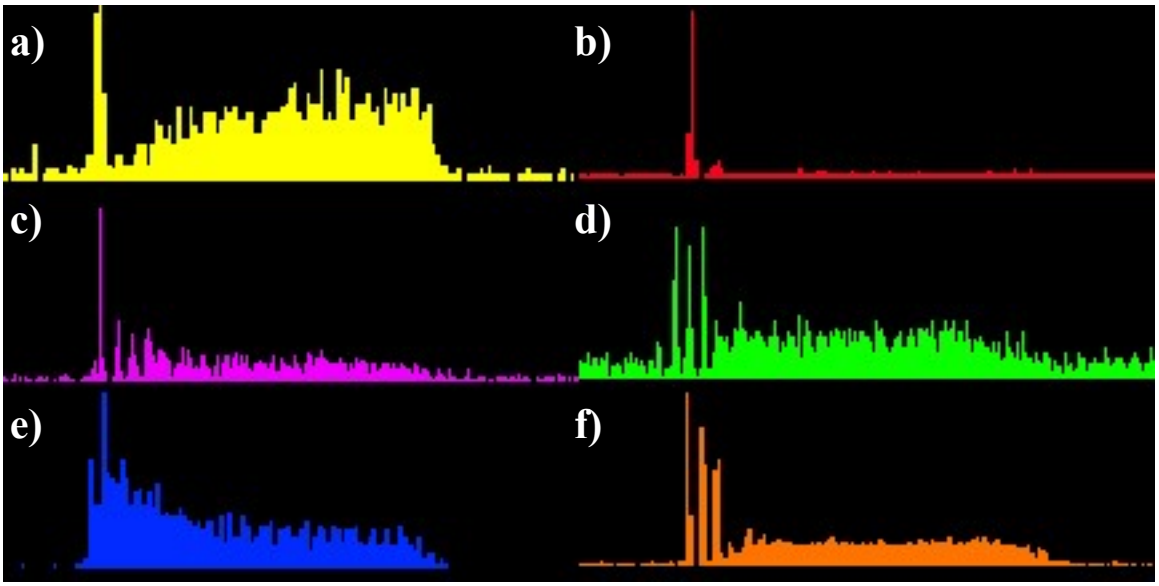



Fig. 7.15: Recorded PSTHs showing DCN a) pauser-buildup, b) onset and c-d) chopper patterns and VCN e) primary-like and f) chopper responses. Note that these PSTHs might not be at the CF of the channel.

### 7.5.2 Recordings and Histology for Probe Placement

The surgical approach enables direct visualization of the DCN probe shanks penetrating the domed surface of the dorsal cochlear nucleus. However, the VCN shanks pass through intact tissue before reaching their target which is more ventral and farther rostral than the DCN. Therefore, it is critical to verify with other methods that these electrode sites indeed reach their intended mark.

One method of verifying the probe location during *in vivo* work is to use the neural recordings themselves. One of the predominant AVCN cell types (spherical bushy cells) exhibits a primary like (PL) poststimulus time histogram (PSTH) at its characteristic frequency (CF), as shown in Fig. 7.16. This differs from cells (globular bushy cells) in the adjacent posterior ventral cochlear nucleus (PVCN) which have a primary like with notch (PLn) histogram. Both PL and PLn responses are significantly distinct from characteristic DCN build-up patterns. During implantation, these differences were used to examine the recorded PSTHs and estimate probe position. However, this method can be difficult to implement for three reasons. First, the cell types, rather than being strictly confined to particular regions, taper off in density as one passes from their primary location to adjacent regions (in particular globular bushy cells). Therefore, an electrode could be physically located in a particular anatomically defined region but still find a cell which is not the predominant type of that region. Secondly, recordings may be multi-unit, perhaps consisting of both PLn and PL cells or of one cell type but with different CFs. Thirdly, the particular indentifying "fingerprints" of a cell's PSTH may only be visible at that cell's CF as well as at a certain stimulus ranges. Thus, if the acoustic stimulation is off of the CF, the expected PSTH will not necessarily be apparent. These challenges made verifying the positions of the VCN probes difficult with respect to the subdivisions, namely the PVCN and AVCN. Therefore, other methods for determining probe location were also used.

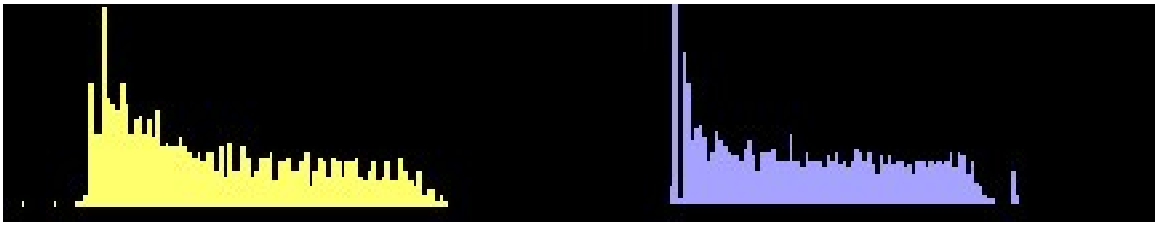


Fig. 7.16: Recorded PSTHs which exhibit PL (left) and PLn (right) characteristics.

A second method for site localization involves marking the tissue during or immediately after the experiment and sectioning the tissue after the experiment to determine the probe location during the experiment. One tissue marking method is to dip the array in fluorescent Fluoro-Gold (FG) dye prior to insertion and thus stain the tissue; this was used in the preliminary mock-up work as detailed in the preceding chapter. The tissue can also be marked with electrical current. One or a few sites can be used to create an electrolytic lesion with this procedure and then the position of the remaining sites can be extrapolated. Both of these tissue marking techniques were employed on the 3-D arrays. Subsequent sectioning, performed by S. Dehmel, confirmed that the sites are reaching the anterior subdivision of the VCN as desired for these studies; one set of marked images is shown in Fig. 7.17. An electrolytic lesion can be used in the VCN also.

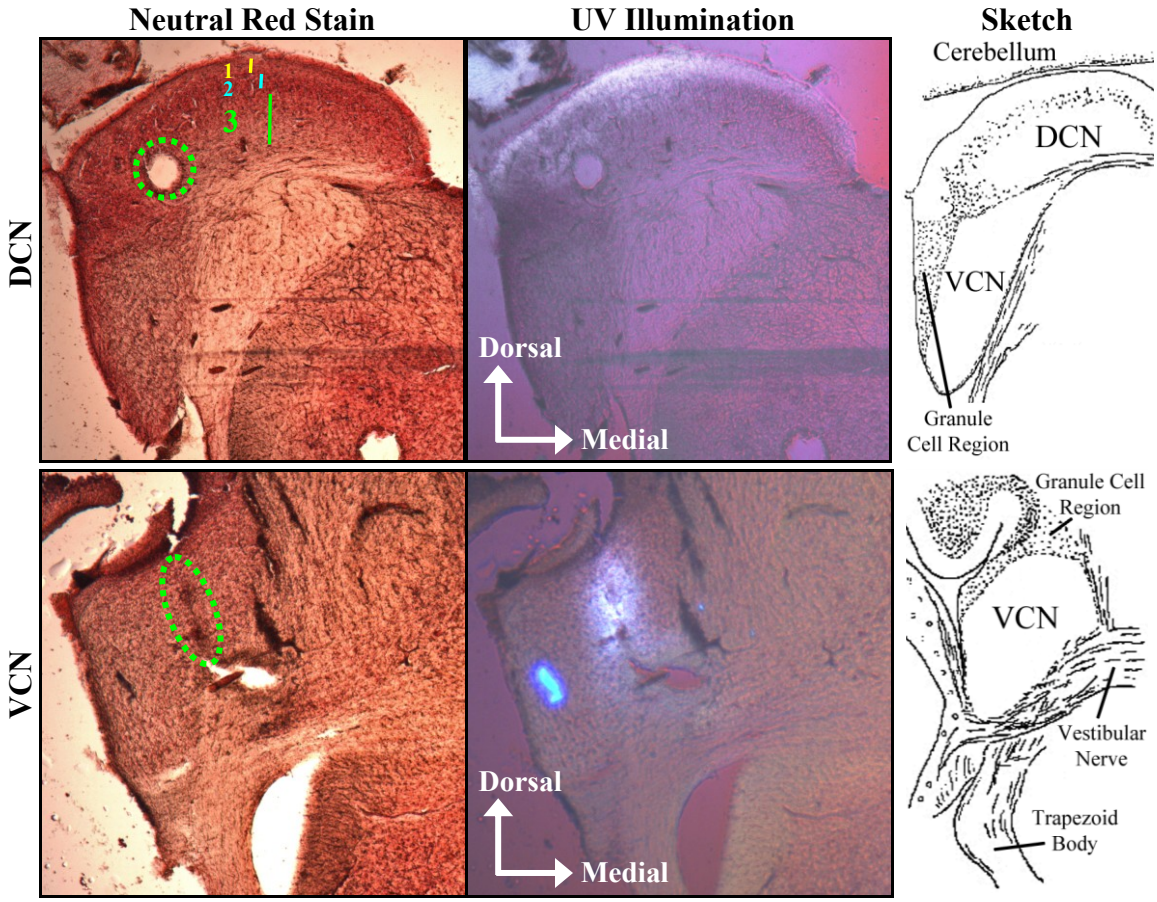



Fig. 7.17: Transverse sections for identifying 2-probe array location from [125] with sketches of similar sections modified from [126]. The current lesion was made using the ventral-most lateral electrode site in DCN (left) and the Fluoro-Gold marks in VCN were from a probe in the lateral-most array slot (right). The sections and analysis were done by S. Dehmel.

### 7.5.3 Threshold and Characteristic Frequency

A typical recording endeavor with acoustic stimulation utilizes a dual parameter sweep of frequency and sound level (dB) of the acoustic signal and records the PSTH for each channel at each stimulus condition set. On a per channel basis, the group of PSTHs can subsequently be plotted with frequency and sound level along the horizontal and vertical axes respectively. Alternatively, the spike rate may be plotted in the same manner. Either method enables the per channel visualization of the threshold, the lowest stimulus level at which an evoked response is generated, and of the characteristic frequency (CF), the frequency of greatest sensitivity. In this work, most thresholds and CFs were determined using ten repetitions of a 50ms acoustic tone for each stimulus condition set (frequency and sound level). One of the many receptive field maps that were graphed based on recordings with the VCN-DCN arrays is presented in Fig. 7.18.

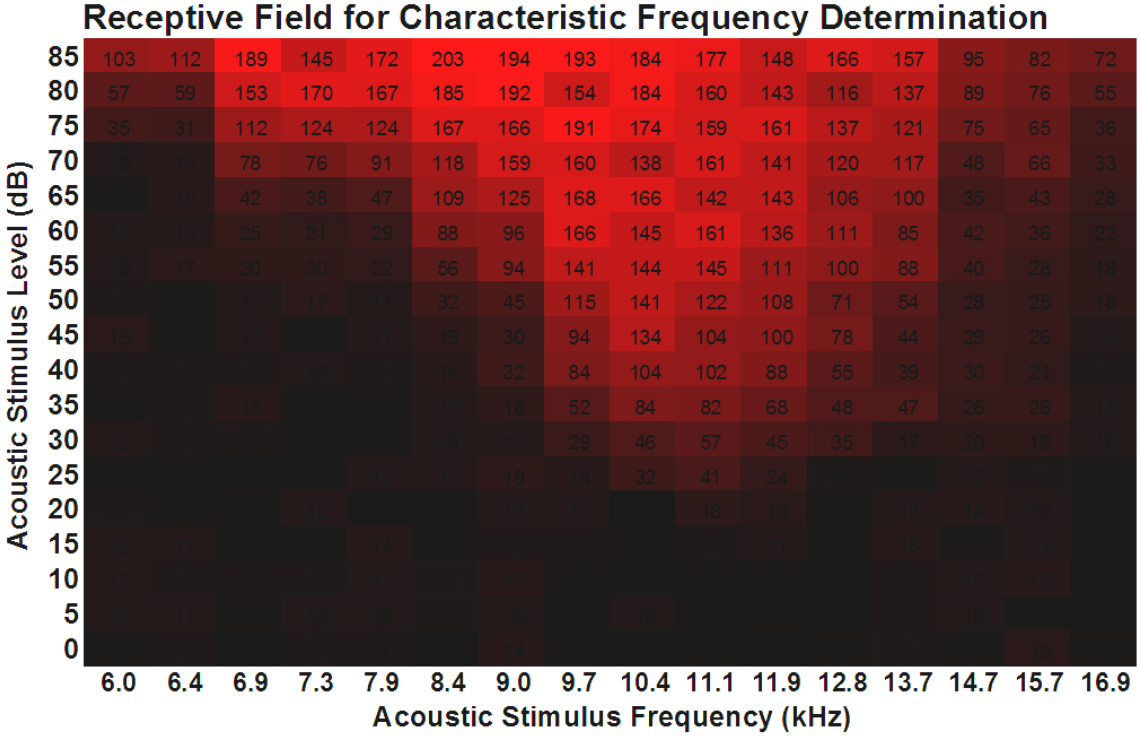



Fig. 7.18: Frequency response map for one electrode site. Each number in the plot represents the spike count for that frequency-amplitude combination. The red-to-black color scale makes the range of responses easier to visualize with bright red and black indicating high and low spike count, respectively.

### 7.5.4 Frequency Maps

It is well known that the CN is organized tonotopically, representing all frequencies that are coded by the incoming auditory nerve. More central locations of the auditory system replicate this tonotopic organization. The tonotopic pattern is evident within each subdivision of the cochlear nucleus complex as indicated in Fig. 7.12. Knowing the correspondence between recording channels and electrode sites, and the relative position of the sites on the probe enables one to plot the CFs with respect to location. Under ideal circumstances, this clearly shows the tonotopic organization of the CN and with future studies may allow greater specificity in locating neurons with particular characteristic frequencies. This also helps during experiments in which multiple regions of the CN are involved since it gives the investigator an intuitive way to visualize if the CFs from which recording is taking place within the two regions overlap each other or are distinct. In some experiments, it is desirable to record simultaneously from neurons with similar CFs in both VCN and DCN. After looking at the frequency map, the researcher knows if the array is properly placed or if it should be repositioned and from knowledge of cochlear anatomy and the measured responses, an indication of in which direction it should be moved. Fig. 7.19 shows CF maps for each electrode location on the probes placed in DCN and VCN.

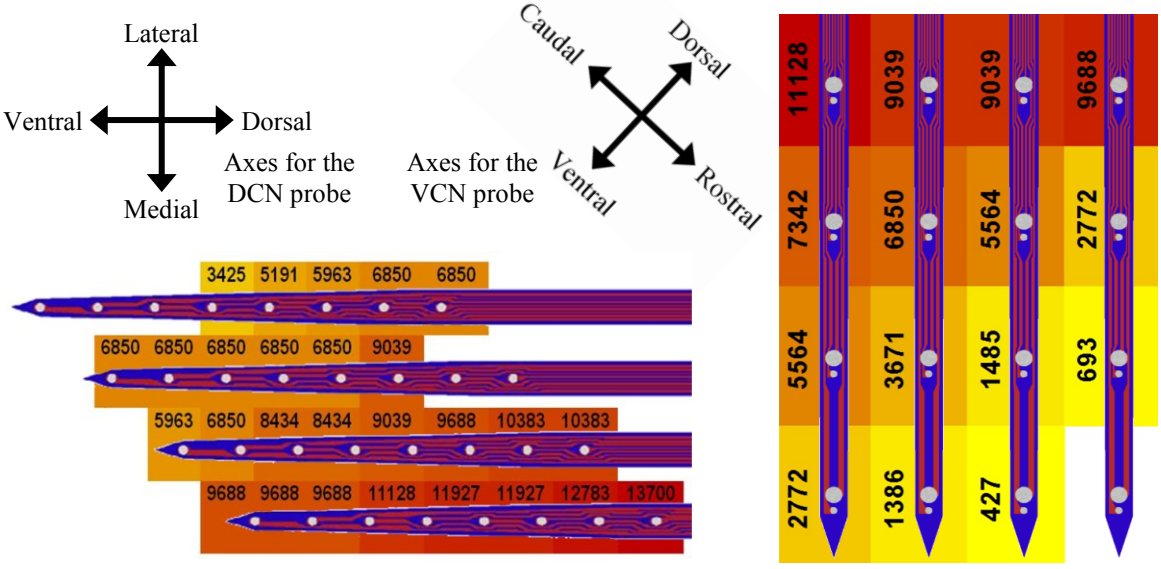



Fig. 7.19: Tonotopic maps of measured characteristic frequency from two guinea pigs, #45 (left) and #40 (right), with separate color scales. The DCN probe (left) is oriented across its medio-lateral tonotopic axis (view from caudal) and the VCN probe (right) is oriented in the dorso-rostral plane (view from medial).

## 7.6 Simultaneous Multi-Region Recordings

The primary purpose of the VCN-DCN array is to record from both CN subdivisions concurrently. This was achieved regularly during *in vivo* work; PSTH and raw waveforms of one such dual recording instance are presented in Fig. 7.20.

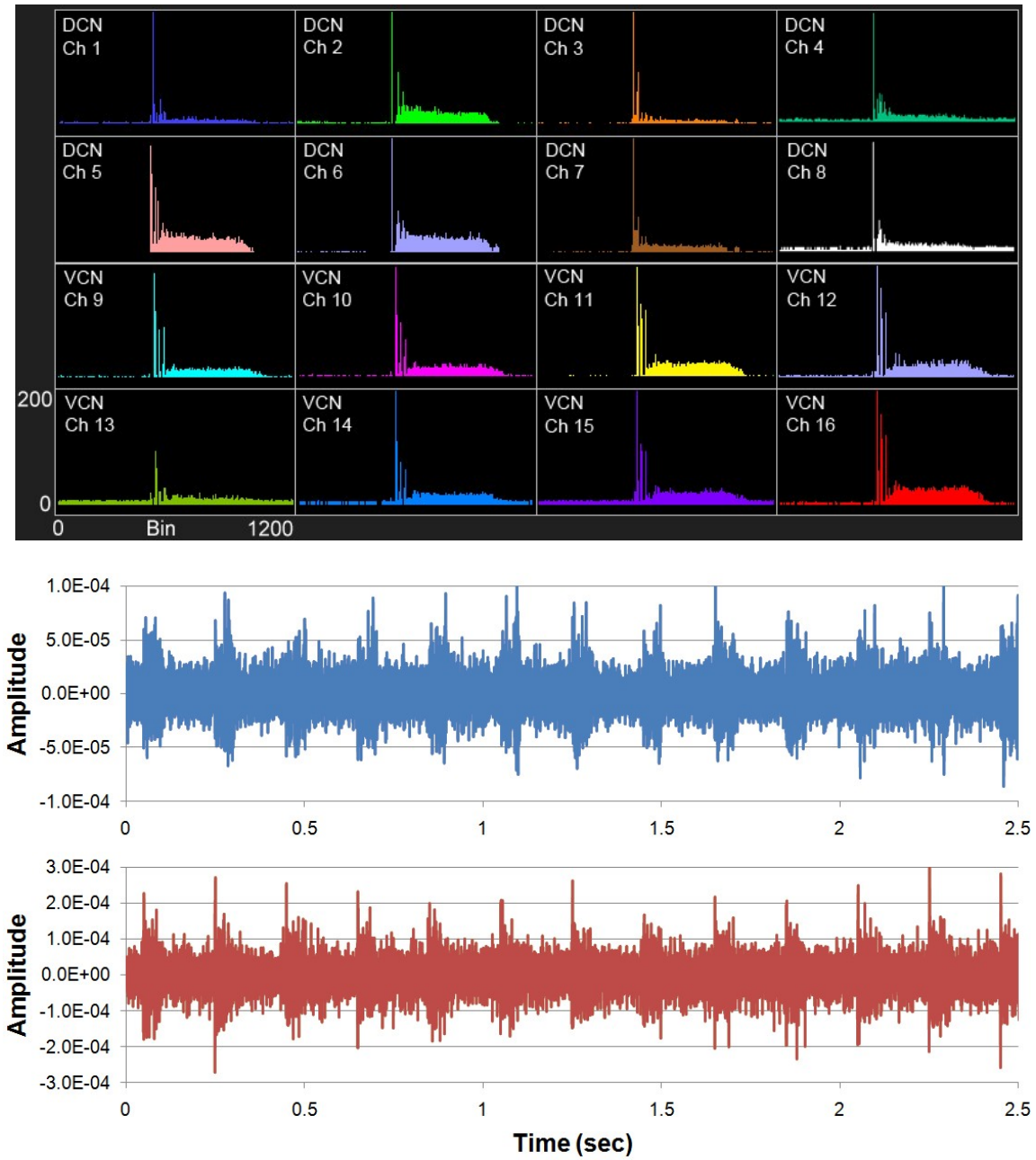



Fig. 7.20: Concurrent DCN and VCN recordings showing PSTHs (top) of selected channels due to the elicited response from acoustic tone bursts at 9688Hz/70dB and raw waveforms (bottom) from one VCN (red) and one DCN (blue) channel. The subnucleus classification labels are based on electrode location within the CN.

## 7.7 Somatosensory Integration Studies

The auditory system may process signals coming from self-generated movements and vocalizations of the subject differently than those from an external source. In order to do this, it is necessary that information regarding the position and movement of the body is integrated into the circuitry of the auditory system. It is the somatosensory system which handles signals which involve the position of the body itself. Research has shown connections between the somatosensory nuclei including the spinal trigeminal nucleus (Sp5) and the cochlear nucleus. In one study, a tracer was injected into the CN and Sp5 cells were retrogradely-labeled as shown in Fig. 7.21. Sp5 projections target multiple cell regions and types within both the VCN and DCN subnuclei, and can influence the responses of CN neurons [127, 128], but much is still to be learned about the influence of these inputs on CN function.

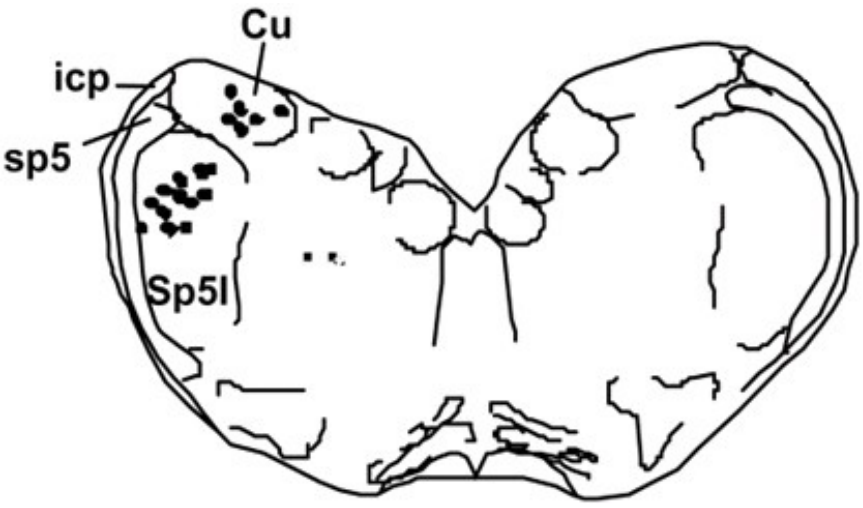



Fig. 7.21: Schematic of a transverse brainstem section showing retrogradely-labeled cells in SP5 after tracer injection into the CN, from [129].

Experiments with the VCN-DCN arrays included investigating the effect of Sp5 connections on auditory coding [125]. Once the CN array was in position, a concentric bipolar metal electrode (FHC, Inc., Bowdoin, ME) was stereotactically inserted into the Sp5 within the same access hole as shown in Fig. 7.22. After determining the characteristic frequencies of the neurons from which recording was taking place, one or more particular acoustic stimulation frequencies were chosen at which to study the multisensory processing.

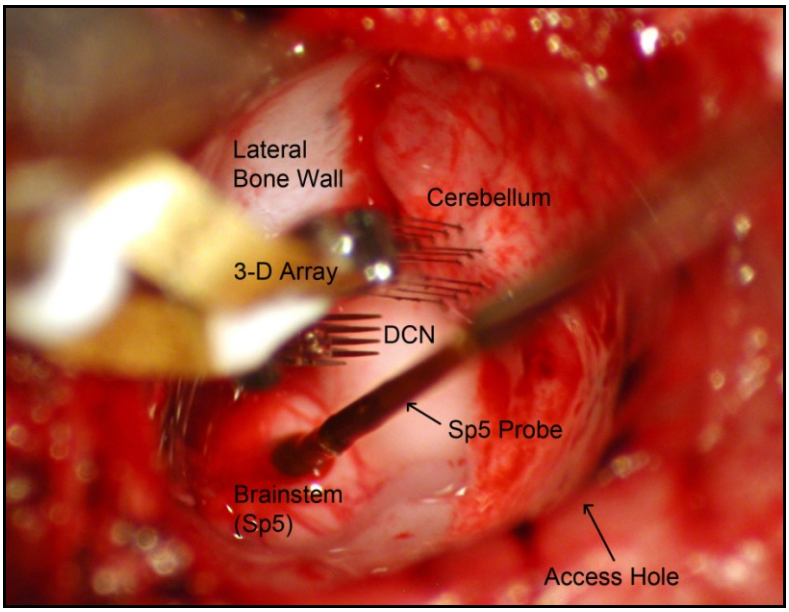



Fig. 7.22: Implanted five-probe 3-D array and Sp5 probe.

The experiment proceeded in three steps. First an initial rate level function (RLF) was recorded with tone stimulation. A rate level function is spikes versus stimulus level; for RLFs in this work, stimulus levels were repeated for fifty repetitions each and changed in 5dB steps. Then Sp5 was stimulated electrically followed 20ms later by auditory stimulation with a second RLF. This was intended to mimic to some extent the condition of the movement/vocalization of the subject (Sp5 stimulation) modifying an auditory-evoked response (acoustic stimulation), thus setting up the necessary situation for the Sp5 inputs to impact the auditory coding. Finally, in order to determine if the Sp5 stimulation had long-term effects, a third RLF was recorded after a thirty minute wait.

Preliminary experimental results indicate that Sp5 projections impact the auditory coding within the CN. As presented in Fig. 7.23, the effect is stronger in neurons that have a characteristic frequency matching that of the acoustic stimulation. For both AVCN and DCN channels, when the CF of a particular channel was at a different frequency than that of the acoustic stimulation, the RLF of some channels showed increased discharge rates and of others showed decreased rates from the initial RLF. However, for DCN channels at the same CF as the tone stimulation, the RLF solely exhibited a decreased discharge rate. This work corroborates with that of [130] which, using a single shank electrode, showed a similar influence of Sp5 stimulation on AVCN channels with CFs matching the tone stimulation.

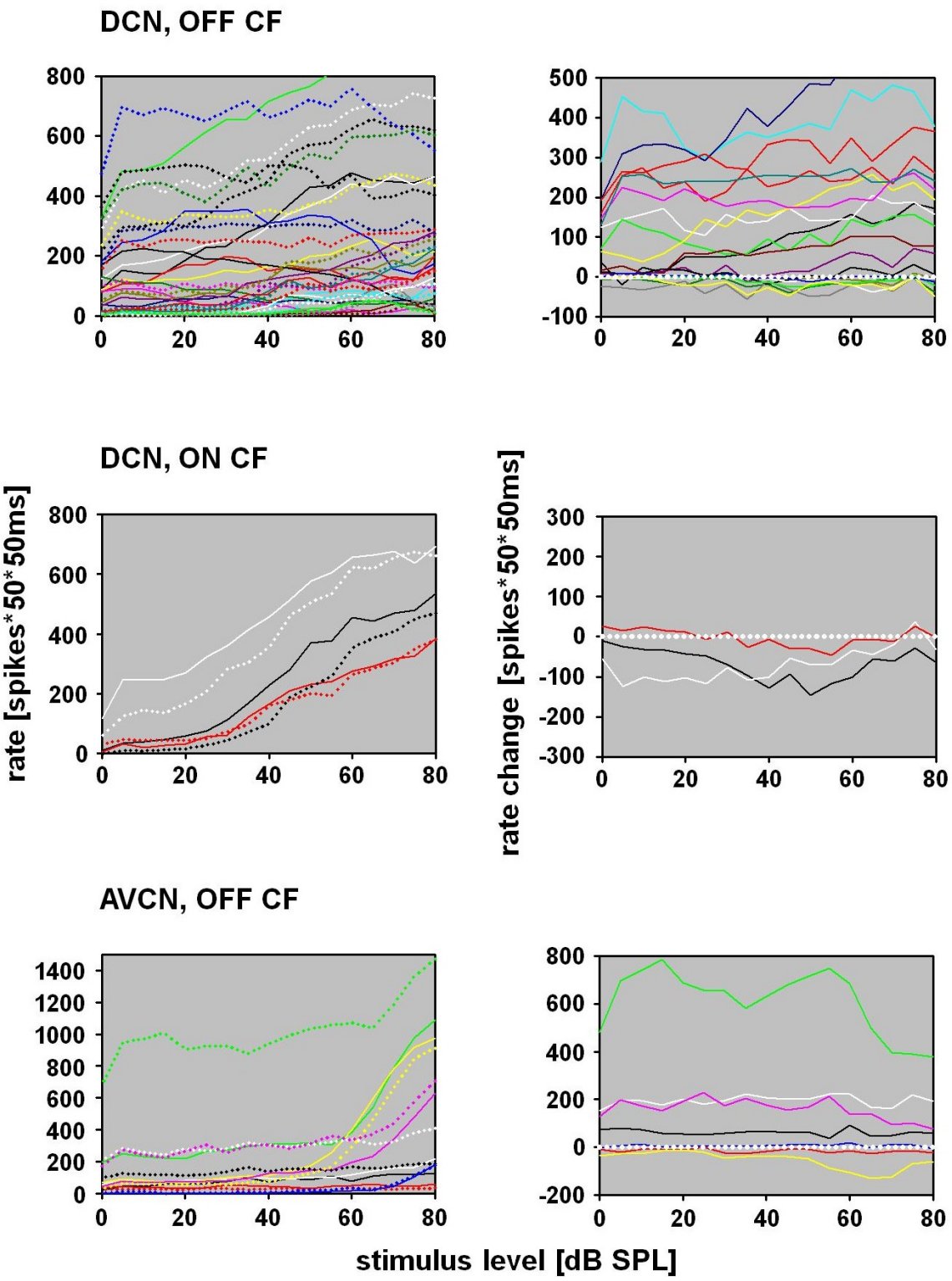



Fig. 7.23: Influence of current stimulation in Sp5 on discharge rates in CN [125]. The left column shows the initial (solid) and final (dashed) rate level functions by recording channel (color) and the right column shows the corresponding difference between the final and initial rate level functions (see text). The graphs are separated by CN subnuclei and CF.

## 7.8 Electrical Stimulation in Neural Mapping

The neural architecture is composed of complex circuits and subcircuits. Anterograde and retrograde tracing studies are the primary techniques employed in the field for determining neural pathways. These techniques enable researchers to follow the projections of neurons down their axons to their target (anterograde) or in the other direction (retrograde), but are limited by injection accuracy, label heterogeneous cell groups (anatomically and neurochemically), and must be evaluated microscopically after the tissue has been prepared (sliced). Electrical stimulation, as a complementary approach, enables studying the living network, from the perspective of particular connections. The basic concept employed is that electrical stimulation can be used to elicit action potentials from neurons near the stimulation sites. These neurons in turn modify the responses of their respective target cells. The neural waveforms of this second cell population can be monitored by recording.

Previous studies have investigated intrinsic pathways within the cochlear nucleus. Planar and radiate multipolar cells in VCN are known to project to DCN [131-135], as illustrated in Fig. 7.24, and so are granule, unipolar brush, and chestnut cells [133]. In some studies, stimulation in AVCN has led to inhibition in DCN [136, 137].

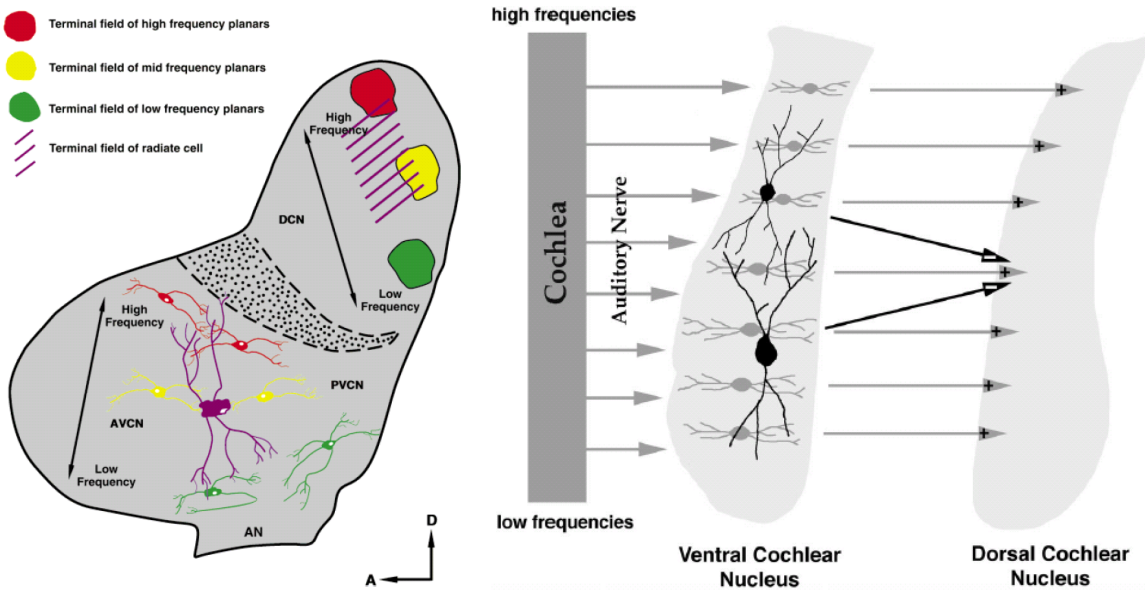



Fig. 7.24: Conceptual drawings of known projections from VCN to DCN, from [132, 133]. Planar neurons (gray), within isofrequency sheets, comprise excitatory inputs to similar frequency DCN sheets. Radiate neurons (black), oriented perpendicular to VCN sheets, project inhibitory inputs in DCN.

In the present work, the bimodal (stimulate/record) approach was used to explore the connections between the AVCN and DCN. Fig. 7.25 shows elicited responses of selected DCN channels after electrical stimulation on one channel in VCN. Graphs a) through c) show similar response patterns with a decrease in spike count immediately after the stimulus followed by significant excitation and then further inhibition. Graph d) exhibits a longer initial period of inhibition (or perhaps two separate periods). Graph e) illustrates a case in which the low spontaneous rate causes the significant inhibition level to fall below zero. Future studies can use broadband acoustic noise or an excitatory neurotransmitter, such as glutamate, to raise the spike rate so inhibition due to the electrical stimulation is visible. Graph f) shows a large stimulus-induced artifact. While artifact was partially removed using an offline sorter, eliminating it altogether would better enable the subsequent analysis of the mapping data. Directions for this include lowering the impedance of the sites, modifying the stimulus waveform and circuits, or using optical stimulation. While further neuroscience experimentation is necessary before conclusions can be made about the connectivity between VCN and DCN channels, the *in vivo* work to date demonstrates the value of high-density electrode arrays tailored to specific anatomical structures, in particular the developed 160-site 3-D VCN-DCN array, for studying the underlying neural circuits.

## 7.9 Conclusions

The VCN-DCN array has not only been used during *in vivo* experimentation which proved its functionality, but it has also contributed to neuroscience research enabling studies heretofore not feasible. Somatosensory integration experiments continue to use this device; the application-specific design permits high-density recording in two CN subnuclei with a commercial stimulation probe in the spinal trigeminal nucleus. On-going studies will focus on the intrinsic connections between the VCN and DCN subregions using bimodal functionality to simultaneously stimulate electrically and record the elicited waveforms. Additional work is being planned to use this array as a prototype for an auditory prosthesis. Not only has this research demonstrated the efficacy of this particular device, it has also pointed the way to support the future of neuroscience research and medical neural prosthetics with bimodal silicon electrode arrays.

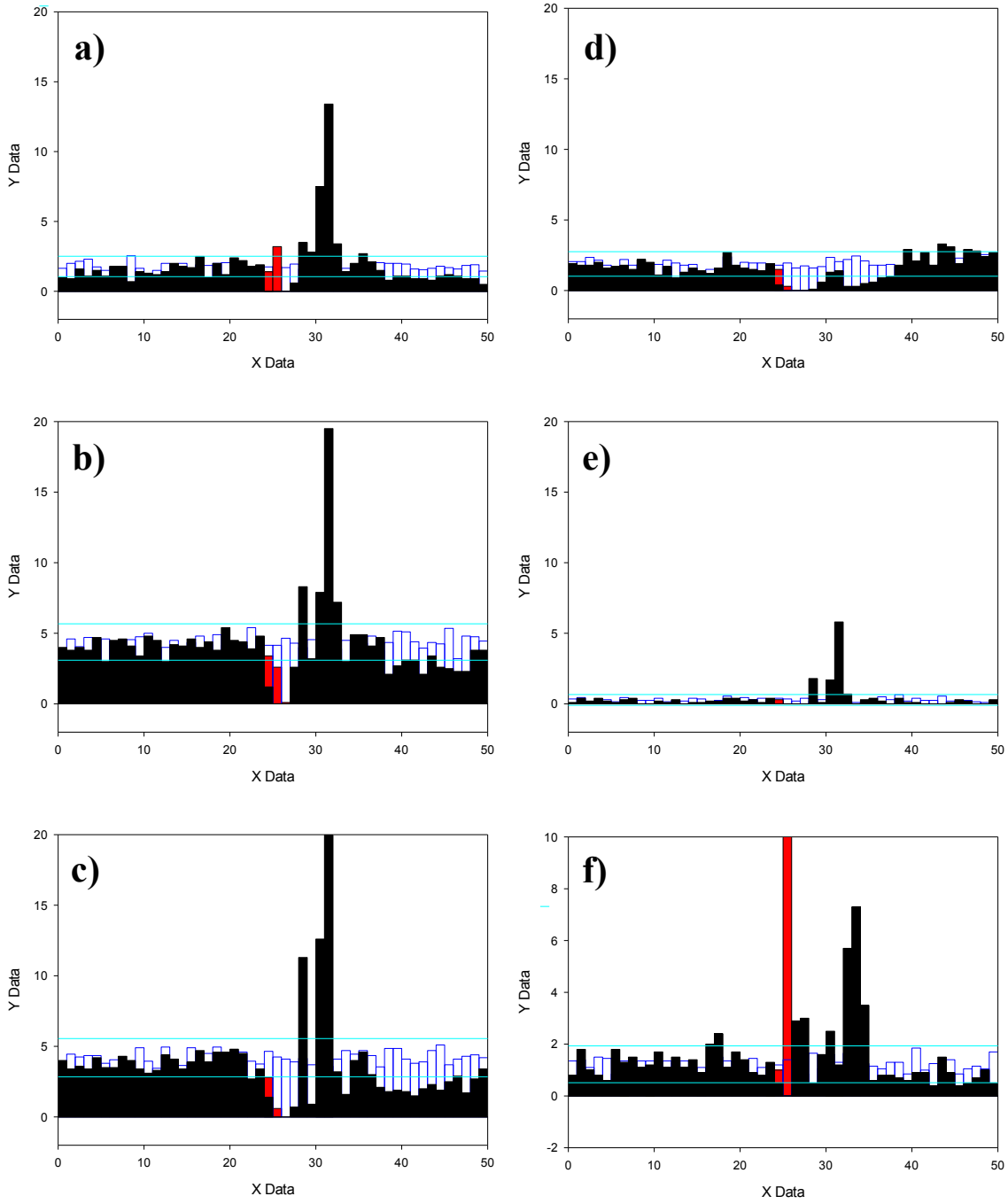



Fig. 7.25: Electrical stimulation on one channel in AVCN elicits neural responses (PSTHs) from selected DCN channels. The stimulus configuration consisted of 50 pulse trains at 20Hz of 10 current pulses each. The pulses were charge-balanced, biphasic, negative-first and at 10μA amplitude. The blue-outlined bars indicate spontaneous rate (measured after the stimulus period). The aqua lines designate 2.86 standard deviations from the average spontaneous rate. The red bars are the sorted stimulus artifact and the black bars are the sorted spikes during the stimulus timeframe. See text for further details.

# CHAPTER VIII

# CONCLUSION

This research builds upon the previous work at Michigan in the development of neural recording and stimulation systems by overcoming critical issues at the front-end of a bimodal electrode array. The developed advances provide scientists with the array architecture necessary to study methods for mitigation of the immune reaction as they work to unravel the complex array-tissue interface challenges inherent in chronic settings. This work also included electrode site modification by the incorporation of carbon nanotubes to decrease site impedance and potentially enhance the chronic neural interface. A low-power low-area recording amplifier was developed to facilitate high channel count systems. Focus on 3-D array design brought about an innovative 3-D array formation method and demonstrated neural mapping with an application-specific array.

## 8.1 Contributions

Within the presented focal areas, the targeted goals were achieved making contributions to the fields of engineering and neuroscience. These include:

- Through chronic (8 week) *in vivo* implantation studies, developed lattice architectures have shown to be an effective means to mitigate the tissue reaction and achieve surviving neurons adjacent to the implanted device.

- To further immune response studies, a suite of fourteen single-shank lattice probes was developed, decreasing implanted shank area with a lattice ($0.064mm^2$) to less than 7.5% of the area of a solid shank ($0.900mm^2$) with the same footprint.

- A novel 3-D array architecture was established which enables probes to be inserted in two perpendicular planes. This architecture and the standard parallel-probe architecture were coupled with multi-shank lattice probes to create, for the first time, 3-D lattice arrays for bio-response investigations.

- Carbon nanotubes were successfully dip-coated and patterned on iridium sites of non-released probes using a photoresist mask. These electrodes achieved an order of magnitude reduction in impedance while maintaining the geometric site area.

- Selective *in situ* growth of CNTs was achieved on iridium sites of non-released probes. This signifies a possible direction for lower impedance, reduced noise, and chronic site stability.

- A low-power small-area neural recording amplifier was designed. Using this circuit within a thirty-two channel system, the amplifiers would take less than $0.9mm^2$ of area and consume less than 1.5mW of power.

- An innovative folding method for forming and rapidly assembling 3-D arrays was demonstrated. This architecture enables the smallest platform structure ever reported for such a device with zero-rise above the top of the platform and virtually no lateral extent past the probe back-ends. The 64-site device stands less than 350μm above the tissue surface and displaces only 1.7% of the instrumented tissue area.

- A three-dimensional application-specific electrode array, one of the most advanced ever reported, was developed for neuroscience mapping studies of the guinea pig cochlear nucleus. This device has permitted, for the first time, high-density 3-D somatosensory integration studies within the CN. It has also demonstrated the efficacy of bimodal silicon arrays in neural mapping through experiments which focused on stimulation in VCN and recording in DCN to further understanding of these neural pathways.

## 8.2 Suggestions for Future Work

The progress achieved points to the value of the engineering contributions in this multidisciplinary field and calls for further collaborative efforts. Work in the following areas would bring this field closer to its full potential:

- The 2-D and 3-D bio-response studies should be continued with uncoated and coated arrays. The studies should also be expanded to include narrow shank designs. Tissue reaction experiments with arrays equipped for recording should be performed.

- Process development for CNT incorporation on released probes should be continued. Accelerated lifetime *in vitro* tests should be performed to evaluate CNT stability. *In vivo* studies should investigate the impact of the CNTs on the recording and stimulation capabilities (noise, back voltage, etc.) and the effect of CNT sites on the chronic immune response.

- Implantable front-end electronics which minimize power and area for a fully wireless bidirectional recording and stimulation system should be integrated with 3-D array technology.

- The 3-D architectures should be employed to place devices in the hands of neuroscientist to use these structures in answering targeted questions about the structure of neural pathways and function of the brain.

# APPENDIX A

# WIRELESS BIDIRECTIONAL NEURAL INTERFACE SYSTEM DESIGN

The system perspective is an important facet of overall design for functional incorporation of individual components. To this end, a bidirectional neural interface system has been designed at the conceptual level. In determining the system specifications, several factors have acted as fundamental guidelines. The application target, a scientific research tool for neural mapping studies, was kept at the fore during design decisions, while also maintaining the possibility for applications of a broader scope, such as neural prosthetics. The aim for the system is an uncomplicated yet comprehensive design. Developments in technology and other previous work at the University of Michigan have been used as a basis upon which to expand. The system design, command word structure and collection, circuit blocks, addressing schema, multiplexing methodologies, fabrication methods, assembly techniques, and other components from previous projects have been reviewed. Drawing from this knowledge and experience base, the current system was fashioned subsuming, when possible and advantageous, structures and developments from prior research. A full command repertoire was devised for complete functionality of the present system along with room for future maturation. The system has also been designed to work with a suite of front-end electrode arrays for increased application flexibility.

While this work focuses in particular on the system front-end, the organization and design of the entire system is also a critical aspect of the research. This appendix presents the complete, envisioned system. The first section briefly highlights the main functionality of the system; this is then expanded upon in Section A.2, which discusses the system commands. Sections A.3 and A.4 set out the system organization with an emphasis on the external components in the former and the implantable circuitry in the latter. Section A.5 introduces three-dimensional electrode array options and Section A.6 discusses site selection capabilities.

## A.1 Functional Overview

This fully wireless implantable microsystem creates a highly flexible neural interface with simultaneous recording and stimulation capabilities as outlined in Table A.1. All power, clock, and control/data signals are sent through a telemetry link. The front-end electrode array features 256 sites distributed on multiple probes arranged in parallel to form a three-dimensional structure. Stimulus waveform generation includes application of a bias voltage and site grounding features as well as electrical stimulation; terms such as "stimulation" or "stimulation channels" are often used to refer to all three of these functions. Due to multiplexing circuitry, each site is capable of both recording and stimulation. The system is equipped with thirty-two recording channels; therefore, a considerable collection of recording patterns are accommodated. Sixteen stimulation channels allow for extensive multipolar stimulation capabilities. During stimulation, a minimum of sixteen recording channels maintain functionality and an additional recording channel is gained for every stimulation channel not in use.

| **Table A.1: System Specifications** | |
|---|---|
| Dimensionality | 3-D |
| Electrode Sites | 256 |
| Recording | 32 Channels |
| Stimulation | 16 Channels |
| Wireless Link | Bidirectional |
| Circuit Integration | 3 IC Chips |

## A.2 Operational Functions and Commands

The bidirectional neural interface system instantiates functionality in three main categories relating to the following:

- recording,
- applied waveforms (stimulation with electrical current, voltage application, and site grounding), and
- circuit and array initialization and management.

Fig. A.1 lists the full command repertoire. The definition of both the command structure and the specific commands was a collaborative process with Dr. Amir M. Sodagar.

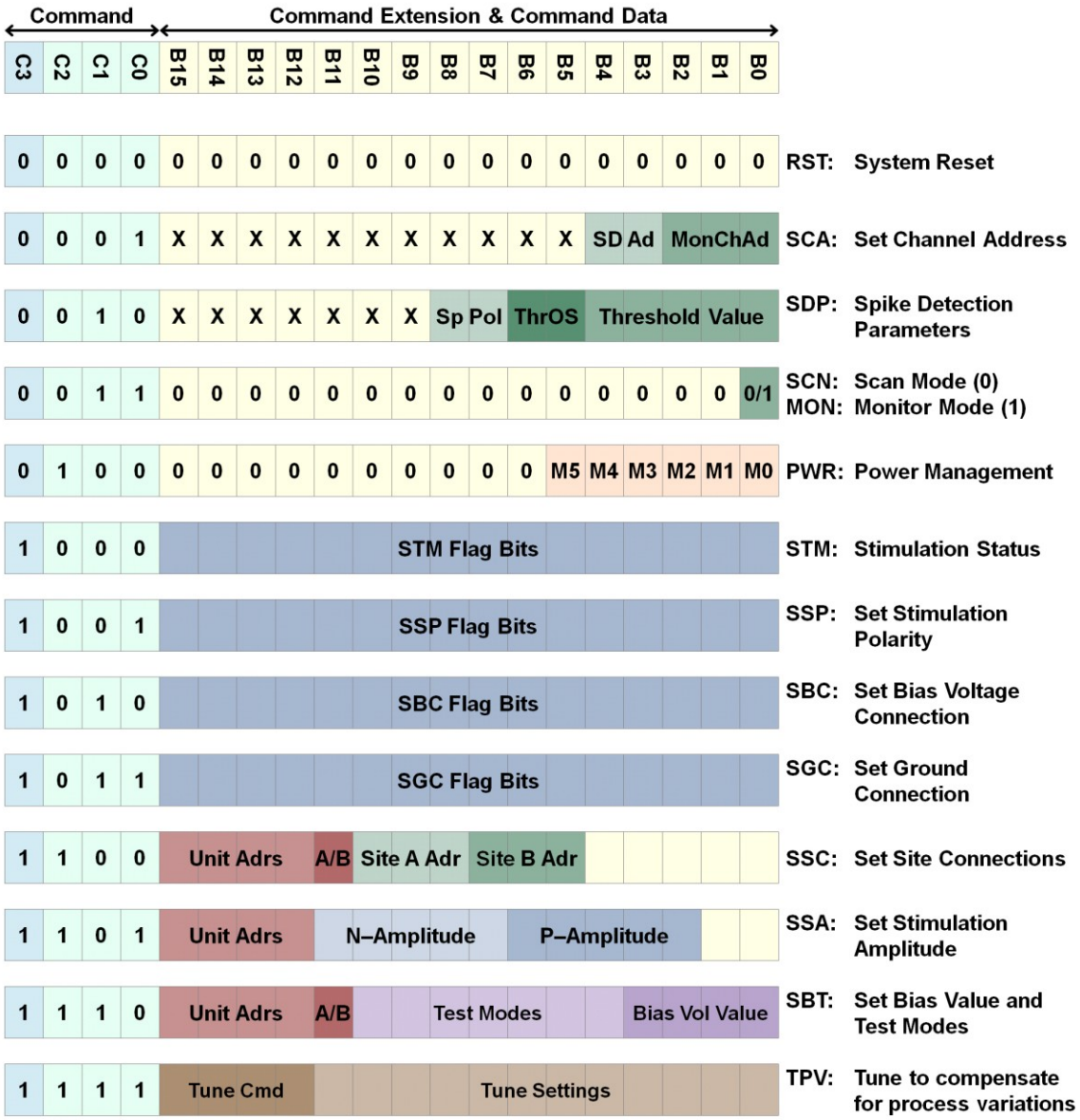



Fig. A.1: Implantable system commands.

In the bidirectional interface, an electrode site may be set to record neural signals or to one of three stimulation options: electrical stimulation, bias voltage application, or site grounding. Thus, the possible circuit connections to any given site are fourfold as

drawn in Fig. A.2. If a particular electrode site is not connected through the multiplexing switches to target circuitry, it is then left floating.

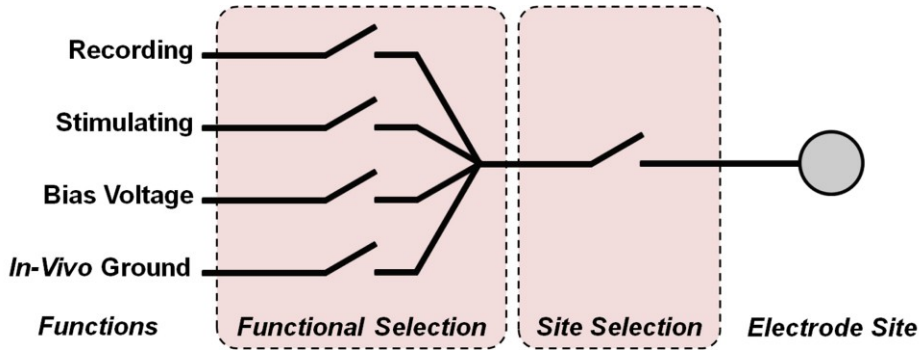



Fig. A.2: Electrode site connection options.

### A.2.1 Recording Related Commands

Two modes of recording operation are offered: Scan Mode and Monitor Mode. For high efficiency of data transfer, in Scan Mode, the system scans the thirty-two channels of pre-conditioned neural signals and transmits the corresponding channel address when a neural spike event occurs. In Monitor Mode, high-resolution eight-bit neural signals on one selected channel are transmitted to the external system. Fig. A.3 illustrates the recording path; the parameters and corresponding commands which must be set for this functionality include:

- selection of the recording electrodes sites (SSC),
- signal pre-conditioning parameters (SBT), and
- recording mode (SCN or MON) and associated settings:
    - the spike detection parameters (SDP) of threshold value, threshold offset, and spike polarity for Scan Mode and
    - channel address (SCA) for Monitor Mode.

Site selection and signal pre-conditioning parameters are detailed further in subsequent sections. The functions of Scan and Monitor Mode given below reflect the work of Dr. Amir M. Sodagar as well as that of previous researchers.

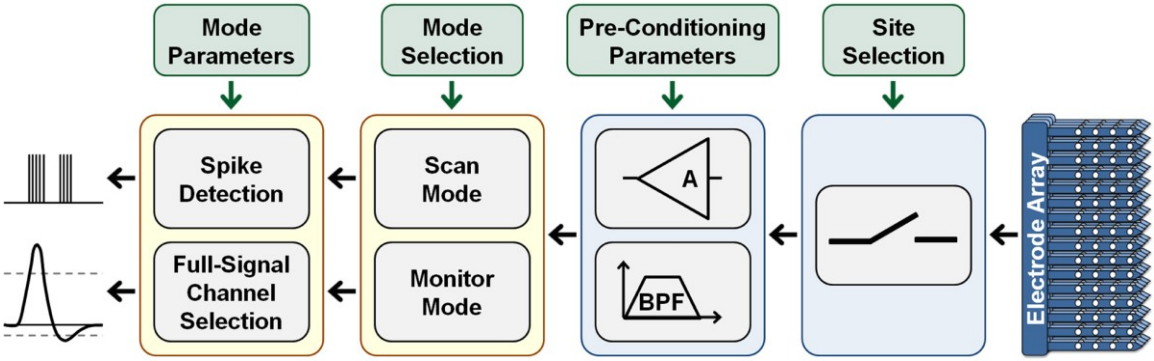



Fig. A.3: Recording path and parameters.

For Scan Mode, the user sets the spike detection parameters (SDP) in order to define the occurrence of a neural spike. Such an event is determined based on thresholding: when a channel is scanned and the recorded signal level is over the set threshold level, the system identifies the channel as having a neural spike. These parameters are set on a per channel basis using the set channel address (SCA) command prior to the SDP command to identify the channel. Three spike polarity options for spike detection are supported: positive, negative, and biphasic as illustrated in Fig. A.4. The two bits reserved for spike polarity (Sp Pol) in the SDP command are active high switches to enable/disable the positive and negative polarity options. When both bits are high, biphasic spike detection is activated. Making both bits low effectively turns off the spike detection on that channel. This is advantageous if a particular channel is not required for a given experiment.

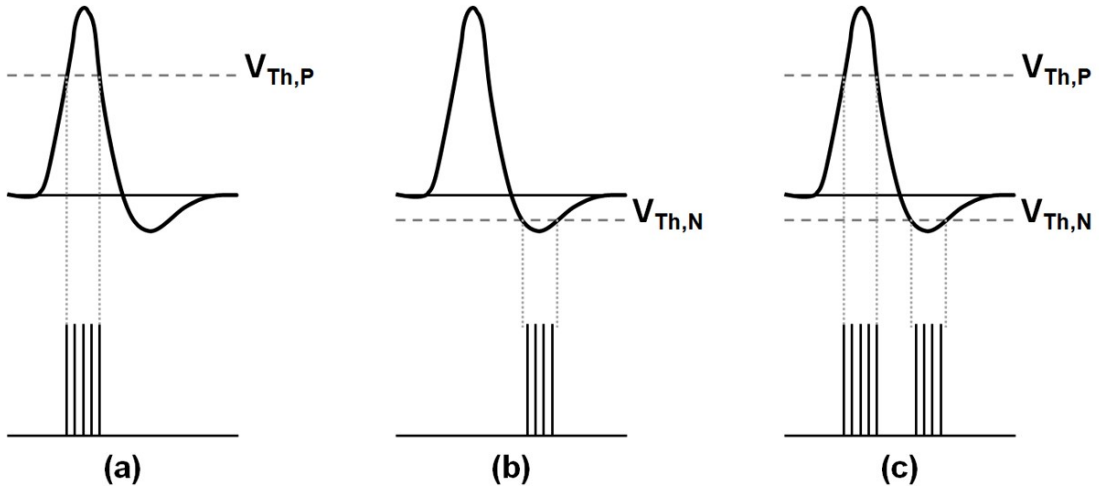



Fig. A.4: The three spike polarity options for spike detection: (a) positive, (b) negative, and (c) biphasic, redrawn based on [138].

The positive and negative threshold levels are defined by the combination of a threshold value (THR) and a threshold offset (ThrOS) as shown in Fig. A.5; both are part of the SDP command. The threshold value is a five-bit parameter in which B0 is the least significant bit (LSB). The threshold offset is a two-bit (three-level) parameter. THR is half of the difference between the positive ($V_{TH,P}$) and negative ($V_{TH,N}$) threshold levels; ThrOS is the midpoint between $V_{TH,P}$ and $V_{TH,N}$.

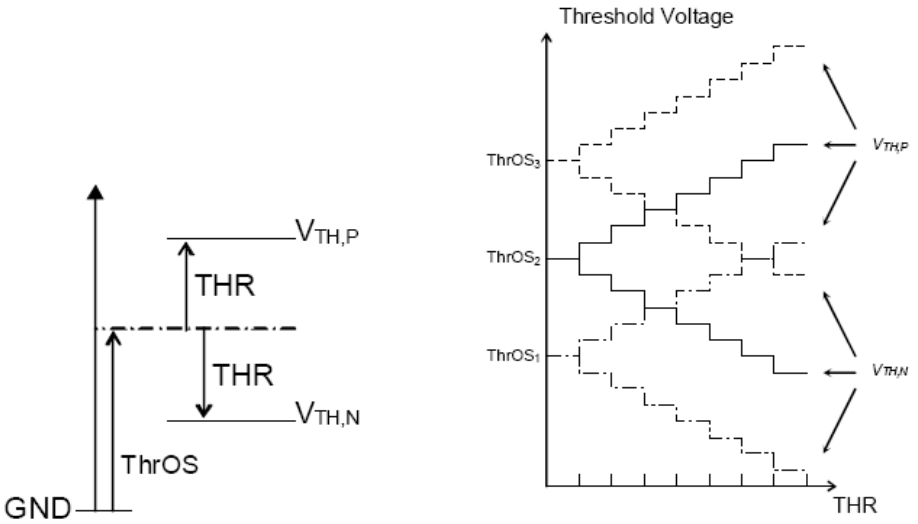



Fig. A.5: The definition of positive and negative thresholds set with a threshold value (THR) and a threshold offset (ThrOS), reproduced from [138].

Considerations have been made to ensure that Scan Mode accurately captures all neural spikes while maintaining their sequence and timing and simultaneously using transmission bandwidth effectively [138]. The thirty-two channels are grouped into four spike detection modules (SD Ad) to enable parallel processing; the eight channels within each module are scanned sequentially. While the amplitude and duration of a spike is not charted in this mode, an estimate of the spike width may be made by the number of sequential times the system reports the channel to be above threshold.

For Monitor Mode, the user specifies one of the thirty-two channels using the set channel address (SCA) command. The module address is specified by the SD Ad bits, in which B3 is the LSB, and the channel within that module is designated through the monitor channel address (MonChAd) bits, in which B0 is the LSB. In this mode, the pre-conditioned analog signal for the selected channel is converted to an eight-bit digital signal and transmitted for viewing and analysis.

A test feature (Trec) for the reverse path is instantiated in the command repertoire as part of the SBT command. When this bit is active, the selected channel is disconnected from the electrode array and a test signal is applied to the channel input, which is the input to the pre-amplifier. This allows for the testing of the amplifier as well as the rest of the reverse path. In addition to amplifier characterization, this feature is useful in determining whether a reduction in neural signals is due to an actual decrease in neural activity or due to a circuit or system issue.

### A.2.2 Applied Waveform Commands (Stimulation, Voltage Application, and Grounding)

Applied waveform commands include biphasic stimulation ability as well as bias voltage application and site grounding features. Four of the commands related to these features have been selected as commonly used functions. This group of commands, termed the Fast Setup commands, enables rapid communication of information for all stimulation channels simultaneously. The remaining applied waveform commands support associated parameter setting. In the next section, both groups of commands are introduced. The subsequent section gives several examples employing these commands to achieve a variety of stimulation waveforms.

#### A.2.2.1 Fast Setup Commands and Associated Parameters

The four Fast Setup commands: stimulation status (STM), set stimulation polarity (SSP), set bias voltage connection (SBC), and set ground connection (SGC) have been expressly designed to enable concurrent command function initiation and termination for all stimulation channels. These commands are based on a flag structure; each of the sixteen data bits for these commands represents one of the sixteen channels. When a Fast Setup command data bit is active, then the associated channel is set to the command function.

Additional settings for the stimulus waveforms include site selection capabilities, stimulation amplitude, and bias voltage value. With multiplexing circuitry, each stimulation channel can access any one of sixteen electrode sites. Further details on site selection are delineated in Section A.6. Stimulation amplitude settings are performed on a per channel basis with the capability of setting both a positive and a negative amplitude.

This allows for fast changes between stimulation polarities even when using non-symmetrical pulses. Due to the flag structure of the Fast Setup commands, the polarity may also be selected on a per channel basis. The magnitude of the stimulation current is set by a five-bit binary word which varies the current from 1μA to 31μA in 1μA steps. There is one bias voltage for the system set with a four-bit code. The voltage range covers ±0.98V in 0.14V steps to enable optimal use of the water window as well as to provide a foundation for exploratory studies on bias voltage application. Bit B15 of the set parameter value (SBT) command sets the polarity for the bias voltage (high is negative); bit B14 is the most significant bit of the voltage value.

The commands and parameters associated with the stimulus waveforms are outlined in Table A.2. Bits are active-high unless otherwise specified.

**Table A.2: Commands and Parameters for the Stimulus Waveform Functions (Stimulation, Voltage Application, and Grounding)**

| Function | Command/Parameter | Description | Scope |
|---|---|---|---|
| **Stimulation** | Stimulation status (STM)* | Initiates (1) and terminates (0) stimulation | Flag bit per channel |
| | Set stimulation polarity (SSP) * | Causes stimulation current to be sourcing (0) or sinking (1) | Flag bit per channel |
| | Set stimulation amplitude (SSA) | Fixes the values of the sourcing and sinking current | Positive and negative amplitudes per channel |
| | Set site connections: stimulation site address (SSC: Stm Site Adrs) | Selects one site out of sixteen for stimulation | Per channel |
| **Bias Voltage Application** | Set bias voltage connections (SBC) * | Links (1) and unlinks (0) channels to bias voltage line | Flag bit per channel |
| | Set parameter values: Bias voltage value (SBT: Bias Vol Value) | Establishes the value of the bias voltage | One value for the system |
| **Grounding** | Set ground connections (SGC) * | Ties (1) and unties (0) channels to *in vivo* ground line | Flag bit per channel |

* Part of the Fast Setup command group.

### A.2.2.2 Example Use of Stimulation Commands

This section contains four examples which use the stimulus waveform commands and present commands details. However, in actual system use, the user interacts with the computer interface and these specifics remain behind the scenes. Nevertheless, a better understanding of system ability will ensue from an awareness of these particulars.

The first commands transmitted are often associated with setting parameter values. For the following discussion, assume that the settings shown in Table A.3 are established before each example begins. These commands can be performed in a setup phase before an actual experiment. Presume also that all four Fast Setup commands are sent with all flag bits set to zero prior to the examples below.

**Table A.3: Initialization Values for Example Stimulation Scenarios**

| Command | Description | Initialization Value |
|---|---|---|
| SSC | Set Site Connections | Site connections have been established for all channels |
| SSA | Set Stimulation Amplitude | All channels have been set with a positive and a negative stimulation amplitude of 16μA. |
| SBT: Bias | Bias Voltage Value | The value of the bias voltage has been set to +0.5V |

**Stimulation Example One**

For the first simplified example, consider the command sequence given in Fig. A.6 during which channels one and two are used for biphasic stimulation.

During the main phase of the experiment in Example 1, two Fast Setup commands (STM and SSP) are used to control the applied waveform. This enables short duration biphasic pulses to be used. In the example code, the initial command (received and implemented at time 0), SSP, sets the stimulation polarity for each channel without actually commencing stimulation. Then the subsequent command, STM, initiates stimulation on channels one and two as shown in Fig. A.7. The successive SSP commands dynamically modify the current polarity while stimulation continues. Due to the flag structure of the Fast Setup commands, multiple channels may be altered simultaneously. For example, command three changes the polarity of channel one from negative to positive and the polarity of channel two from positive to negative. If a

particular channel does not need settings changed when a command is transmitted, then the bit setting required to maintain its functionality is used. This is demonstrated in command four; the polarity flag of channel three remained the same as in the previous SSP command. The final STM command is used to terminate the stimulation.

| | Flag Bits for Stimulating Channels | | | | | | | | | | | | | | | | Command | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSP: | Set Stimulation Polarity |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | STM: | Stimulation Status |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SSP: | Set Stimulation Polarity |
| 3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | SSP: | Set Stimulation Polarity |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | SSP: | Set Stimulation Polarity |
| 5 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STM: | Stimulation Status |

Fig. A.6: Example 1 stimulation command sequence. The number on the left indicates the time step at which the command was implemented.

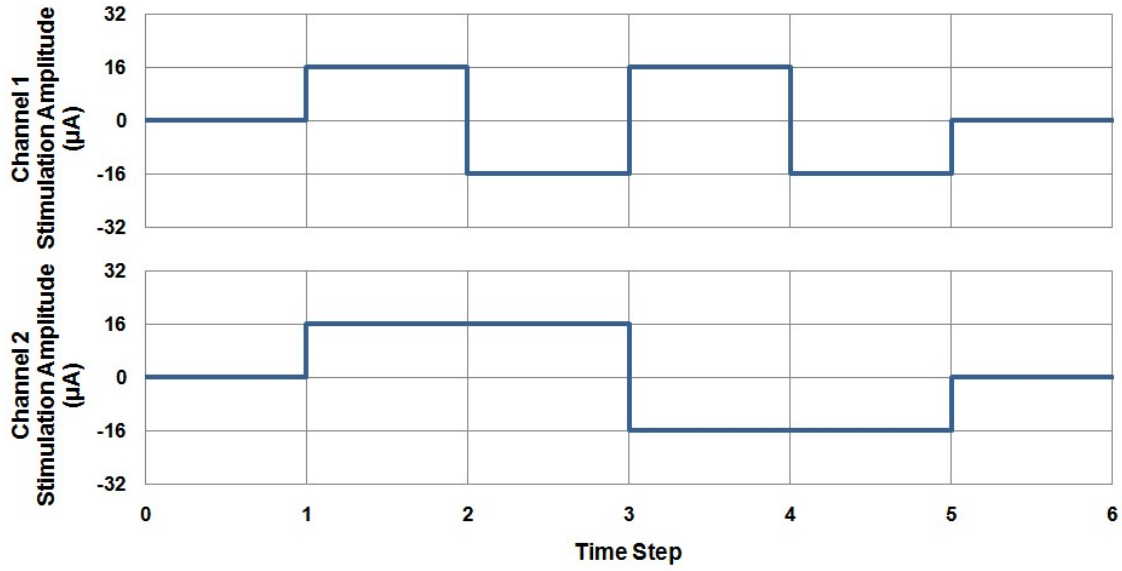



Fig. A.7: Waveforms corresponding to the command sequence for Example 1.

The minimum time step is determined by the least possible time between two sequential commands; in other words, the minimum time step is equal to the delay of transmitting one command. This interval, in turn, is established by the system clock speed and the number of bits that must be sent per command. As discussed below, the full wireless system uses a twenty-seven bit word including the start pulse and parity bits. Thus at a 2MHz clock rate, the minimum time step would be as short as 13.5µs. The effect of this time step on the case at hand would mean that channel one is delivering symmetric, charged-balanced, biphasic pulses with a phase width of 13.5µs and a total pulse width of 27µs. Simultaneously, channel two is stimulating with a charge-balanced phase width of 27µs and thus a pulse width of 54µs. A 2MHz clock rate is considered since the wireless module and signal processing circuitry were both designed for this speed; chip testing may indicate faster rates are possible.

One may use the system to define pulses as demonstrated in Example 1 and then add in an intertrain delay using the STM command as Fig. A.8 shows. Also illustrated on channel one is the use of site grounding (SGC) during the intertrain delay.

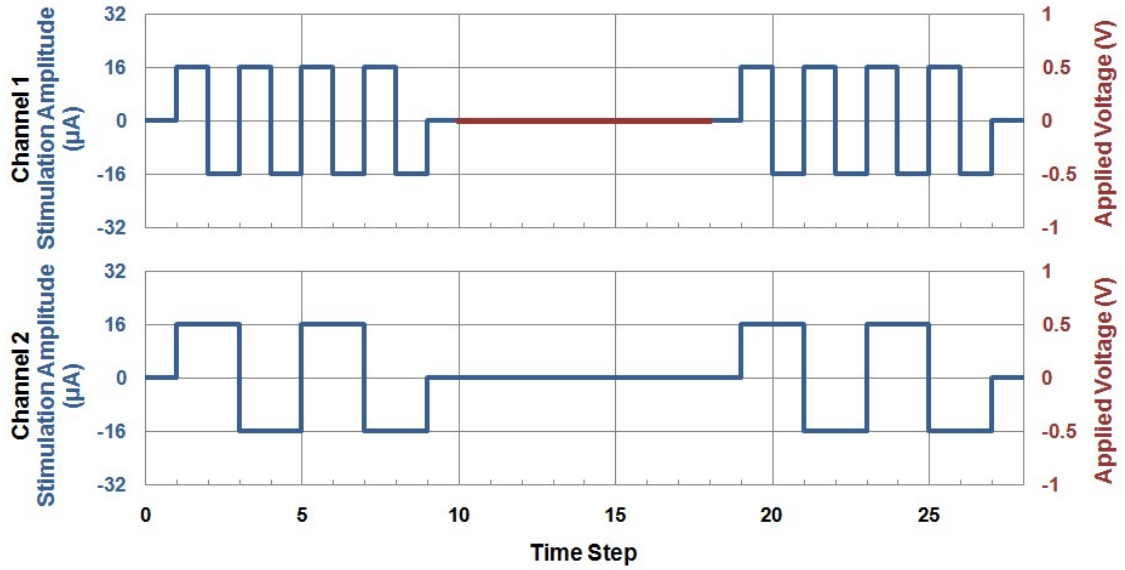



Fig. A.8: Example pulse train waveforms with intertrain delay.

The minimal time step is small compared to typical neural stimulation pulse widths [139-141]. If a longer time step is desired than that required for command transmission, then the LabVIEW interface controls the additional delay between the

subsequent transmissions of commands. For example, the commands could be sent at intervals eight times the minimum, that is, at 108μs intervals. This would result in a biphasic pulse width of 216μs on channel one (108μs/phase) and of 432μs on channel two (216μs/phase). Alternately, the extra time may be used to transmit additional stimulation commands to perform functions on other channels as is detailed in the next example.

The constant current stimulation methodology was selected over the constant voltage scheme so that the charge delivered per phase is consistent regardless of the electrode impedance. However, when the electrode sites are dual-function (record and stimulate) there is a trade-off in the design decision of electrode size. Stimulation sites of past systems had an area of $1000\mu m^2$. To record single units, electrodes with a geometric area of $177\mu m^2$ or less are typical. This area corresponds to significant electrode impedance, on the order of megohms, which is impractical for large amplitude electrical stimulation with low voltage supplies. The site size/impedance design challenge can be approached from two sides. The first is to increase the effective site area while maintaining the geometric area through the use of electrical activation of the iridium electrodes to form iridium oxide and/or through the incorporation of carbon nanotubes on the site surfaces, or similar methodology. The second strategy is to enable the same charge delivery with longer pulses of lower amplitudes.

**Stimulation Example Two**

The four Fast Setup commands enable dynamic modification of frequently used stimulation functions. If all four functions are implemented in a given experiment using multichannel stimulation, it may be advantageous to employ a standard rotation of these commands. With this technique, the timing resolution would be four times the minimum time step, 54μs with a 2MHz clock. Since stimulation pulses are most commonly biphasic in nature, the width of one phase in a symmetric pulse could still be as small as 27μs if the STM and SSP commands were spaced with the SGC and SBC commands. If one of these four commands is not used, then it may be omitted and the rotation shortened further. This method was employed in a second example; an excerpt of the command sequence is shown in Fig. A.9 and waveforms are graphed in Fig. A.10. The following discussion will assume that the time step is the minimum possible.

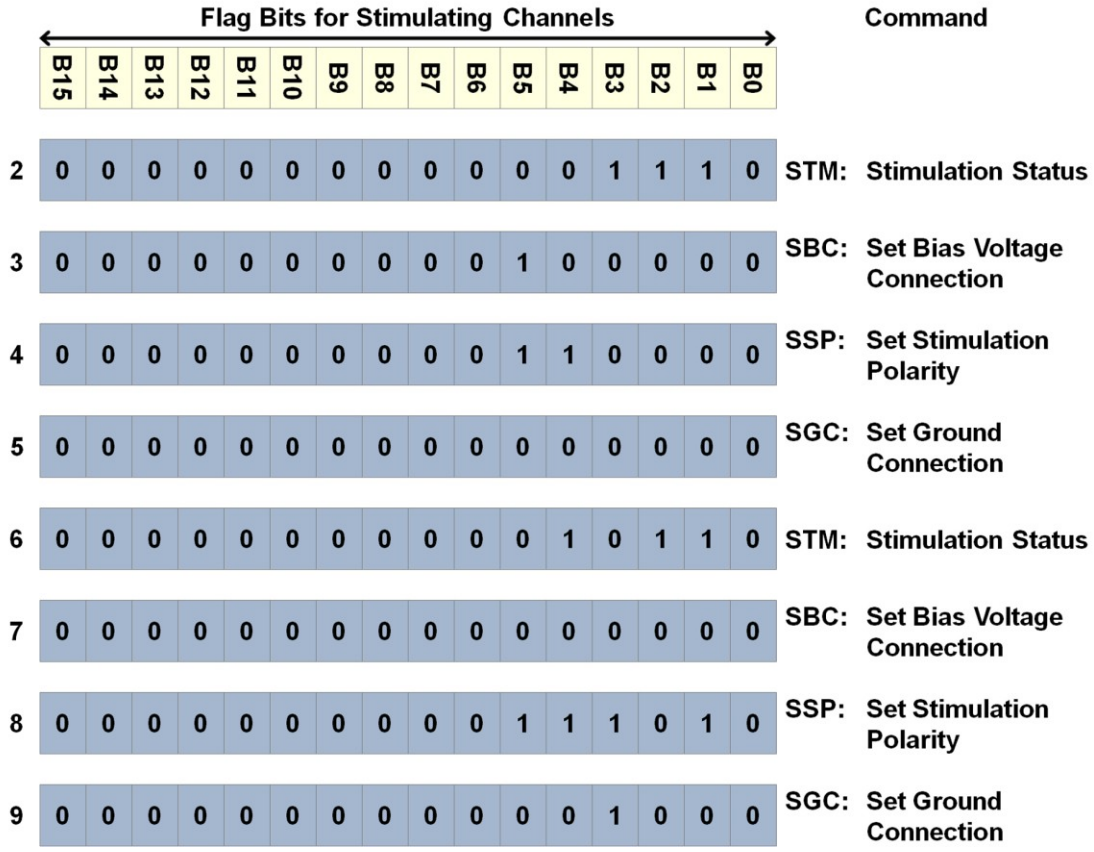


Fig. A.9: Excerpt of stimulation command sequence for Example 2.

Instead of using a delay to set the width of the phases, the Fast Setup commands are sent on a rotational basis and when sent, the flag bits are set to indicate the required states for each channel. This allows considerable flexibility in the waveform shapes and timing as the graphs indicate. While relatively short pulses and intertrain delays are used for example clarity, there is no upper limit on either, although charge balancing is necessary for safe stimulation.

For continuity, channel one and channel two show waveforms similar to those in Example 1; with a 2MHz clock, their widths are 108µs/phase and 216µs/phase respectively. Channel three includes an interphase delay with site grounding; the phase widths on this channel would be 27µs with a 2MHz clock. The fourth channel incorporates an intraphase delay as well as an interphase delay. Channel five employs the bias voltage feature between single phase pulses and temporary site grounding after the conclusion of each pulse train.

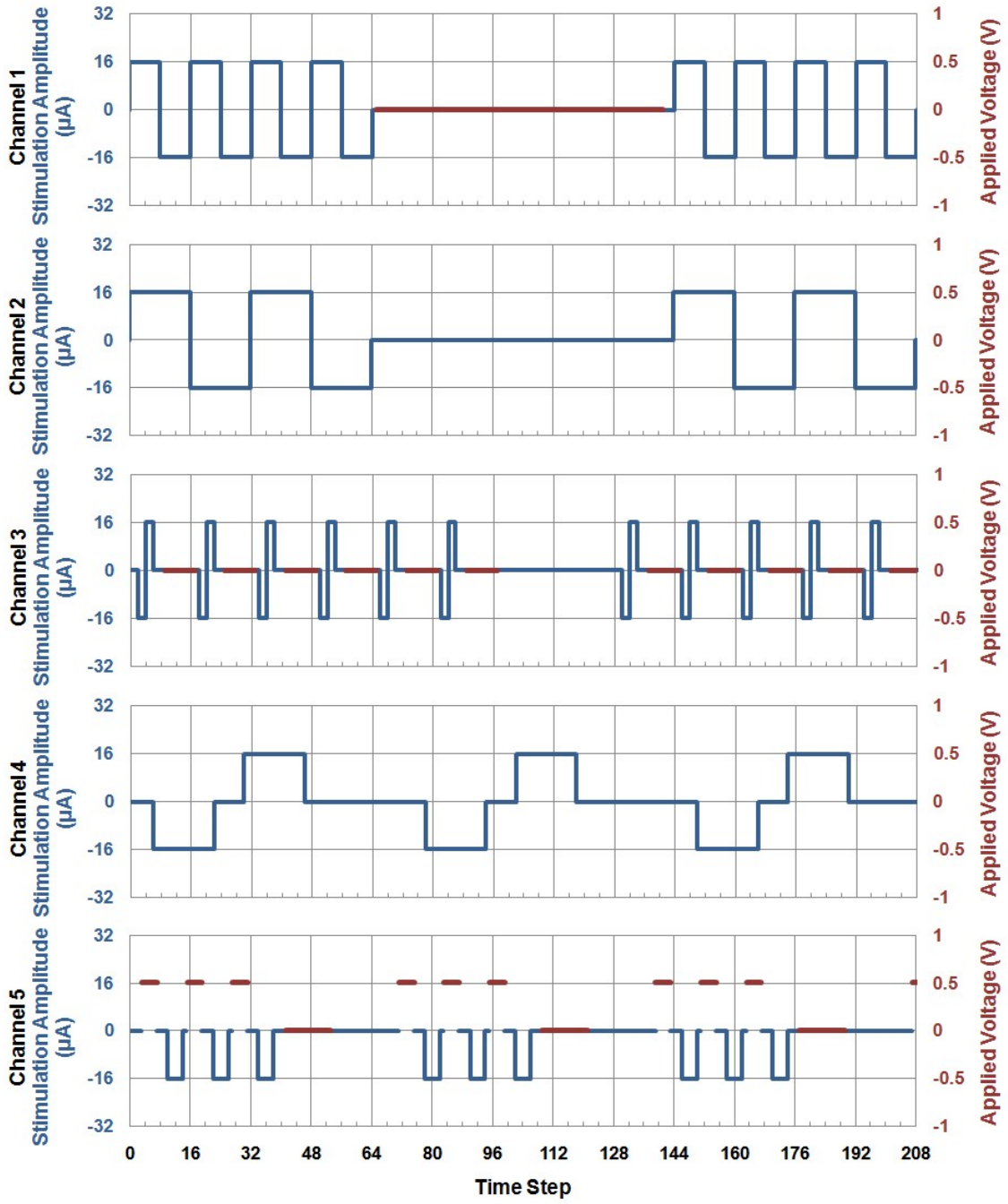



Fig. A.10: Waveforms for Example 2 (1 Time Step = 13.5µs for a 2MHz clock).

**Stimulation Example Three**

While the smallest time resolution is achieved by limiting the commands to the Fast Setup group, the other stimulation commands may still be incorporated in command sequences. This supplements the stimulus waveform functionality with the ability to alter site selection, stimulation amplitude, and bias voltage value.

The most opportune time to include additional commands would be during interphase or intertrain delays when flag settings do not need to be dynamically modified. The scenario graphed in Fig. A.11 utilizes this capability to modify the pulse amplitudes. Selected code for the first two biphasic pulses is given in Fig. A.12. The first two commands are part of the initialization phase and so are not labeled with time steps. This sequence demonstrates that for two sequential, biphasic pulses the shortest interphase delay possible is three times the minimum time step (40.5µs with a 2MHz clock) if both the polarity and amplitude are to be changed during the delay. In order to preserve phase visibility in the graph, the minimum phase width was not used.

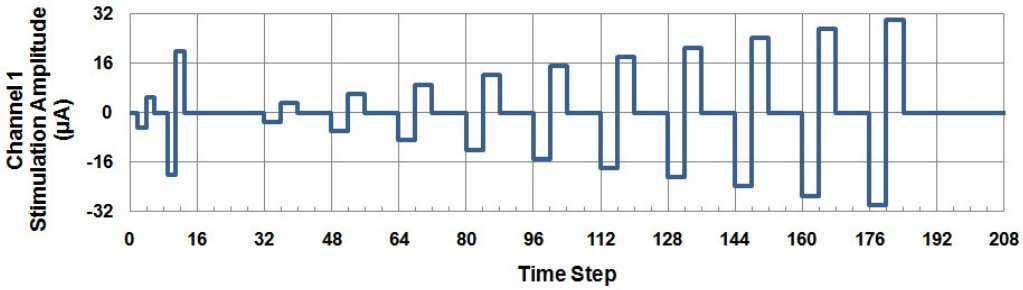



Fig. A.11: Waveform for Example 3 demonstrating use of the SSA command to change the channel amplitude during the interphase delay.

| | Flag Bits for Stimulating Channels | | | | | | | | | | | | | | | | Command | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SSP: | Set Stimulation Polarity |
| | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | SSA: | Set Stimulation Amplitude |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | STM: | Stimulation Status |
| 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSP: | Set Stimulation Polarity |
| 6 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STM: | Stimulation Status |
| 7 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SSP: | Set Stimulation Polarity |
| 8 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | SSA: | Set Stimulation Amplitude |
| 9 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | STM: | Stimulation Status |

Fig. A.12: Command sequence excerpt for Example 3.

**Stimulation Example Four**

The previous examples used symmetric, biphasic pulses. However, since space is reserved for two stimulation amplitudes per channel, one positive and the other negative, non-symmetric pulses may be dynamically created without requiring amplitude alteration during the intraphase delay. The plot in Fig. A.13 displays an example waveform with non-symmetric pulse phases; a selection of the corresponding code is given in Fig. A.14.

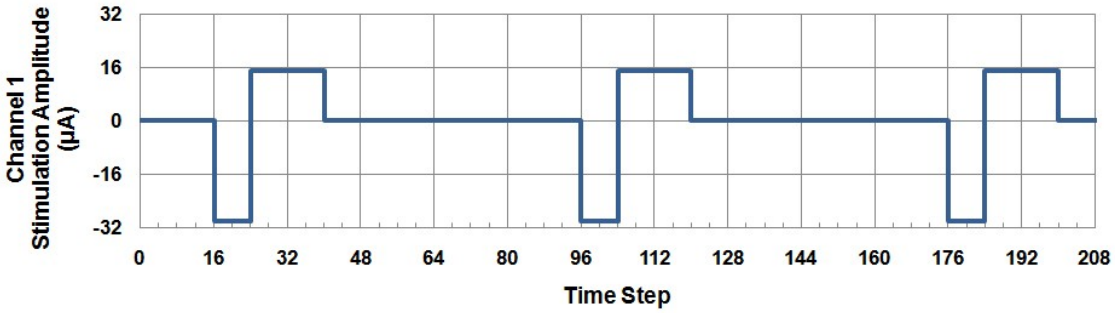



Fig. A.13: Waveform for Example 4 set with different positive and negative stimulation amplitudes during the initialization phase.

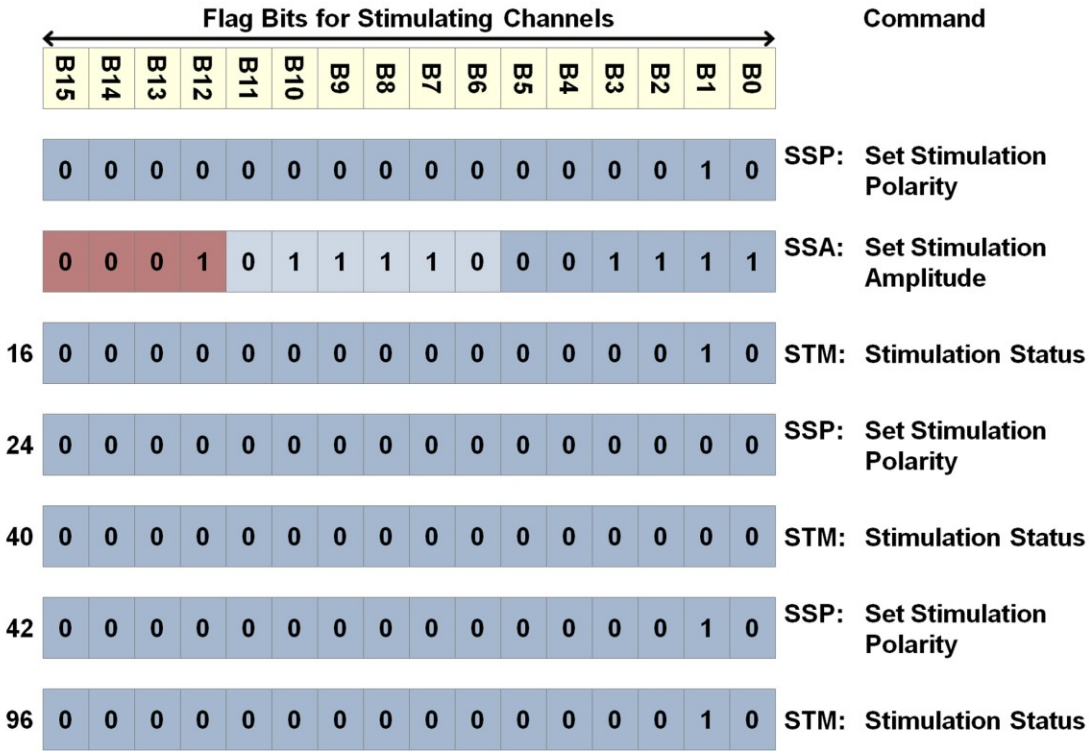



Fig. A.14: Excerpt of command sequence for Example 4.

### A.2.2.3 Test Feature for the Stimulation Path

Stimulus waveform functionality relies on the proper operation of the stimulation circuitry. A test feature (Tstm) is included in the command repertoire as part of the SBT command to assist in verification of this functionality. When the bit is active, the selected channel is disconnected from the electrode array and is fed through test circuitry. The test output is connected to one of the recording channel inputs so that the result can be received by the external system with the use of Monitor Mode.

### A.2.2.4 Synopsis of the Stimulation Related Functions

The command structure and control logic have been designed to enable concurrent stimulation initiation and termination for all stimulation channels. This enables dynamic modification in stimulation parameters such as stimulation polarity, pulse width, and signal timing, as well as in interpulse settings of site floating, bias voltage application, or site grounding. Thus, rapid execution of key commands resulting in a small timing resolution as well as channel synchronization is achieved. At a 2MHz clock rate, simultaneous, charged-balanced, biphasic pulses may be generated from all 16 channels with individually set amplitudes and with pulse widths of 13.5μs/phase or greater. Asynchronous pulse widths and incorporation of bias voltage application and site grounding may be achieved with a 54μs timing resolution. Parameter values such as site connections (one site out of sixteen per channel), stimulation amplitude (1μA to 31μA in 1μA steps), and bias voltage values (±0.98V in 0.14V steps) may be modified during interpulse delays for increased waveform flexibility. A test mode is also incorporated for confirmation of stimulation functionality.

## A.2.3 Circuit and Array Initialization/Management Related Commands

Several initialization and management commands bring the command repertoire to completion. The system includes a standard command for system reset (RST) as well as a command for power management (PWR) with which selected modules may be powered off. Power management bit M0 corresponds to the NPU scan and M1 controls power to the analog to digital converter (ADC). Power is connected to the modules when the bits are high. In addition, the command set includes reserved (RES) space for future development of the system.

The electrode array initialization and management commands are site activation (Act) and site impedance measuring (Timp). In order to electrochemically activate iridium electrode sites to form iridium oxide for improved stimulation ability, the system is placed in site activation mode. In this mode the sixteen stimulation channels are connected in parallel to an external pad through which the activation signal can be applied. The site selection command is used to rotate through all of the sites, which will only take sixteen times in the full 256-site array since sixteen sites are activated simultaneously. Previous work has shown that activating sites in parallel not only significantly reduces the time required for activation but also achieves more uniform iridium oxide [62].

Site impedance is used as an indication of the state of an electrode site and its associated interconnect leads and environment. Before implantation, site impedance is used to verify that leads are properly connected without shorts or opens. It is also used as part of the site activation procedure as an assessment of the stimulation ability of the site in question. Once implantation occurs, the condition of the array, electrode site, and the electrode-electrolyte interface is a critical yet enigmatic aspect of system functionality. If there is a reduction in recorded signals, it is advantageous to have methods for determining possible causes before explantation. While recording characteristics of microelectrode sites may be more directly related to geometric area than impedance, monitoring impedance over time may indicate the occurrence of changes such as tissue encapsulation.

The site impedance measuring feature applies a test signal to the selected electrode site; the output of the test circuitry is routed through the input of one of the recording channels. This enables the system to transmit the results to the external system through the use of Monitor Mode.

## A.3 System Overview

The complete neural mapping system is broadly divided into the external operating system and the implantable microsystem as illustrated in Fig. A.15. The external system comprises the software and hardware required for the user interface and the external portions of the data processing and wireless communication. The

implantable portion of the system is composed of circuitry which supports wireless operation, internal data processing, and other central aspects of system functionality, and of MEMS structures which form the physical arrangement of the internal components and the direct interface with the neural tissue.

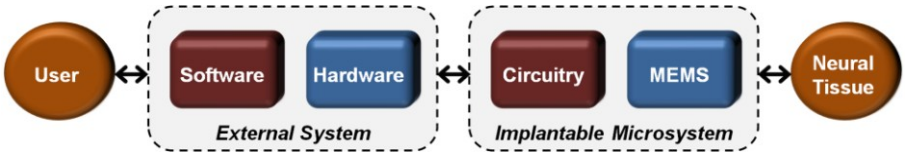



Fig. A.15: Simplified system overview.

### A.3.1 External System

The external system acts as the intermediary between the user and the implantable system as shown in Fig. A.16. To enable ease of use, the operator interacts with the external system through a graphical user interface (GUI) implemented as part of a National Instruments (NI) LabVIEW Virtual Instrument (VI) software program. The LabVIEW program also handles the data preparation and processing, which includes packet generation for the forward telemetry path (passing of signals to the implantable microsystem, also termed "incoming" path) and packet check, data extraction, and data translating and formatting for the reverse direction (recovery of signals sent out from the implantable microsystem, also called "outgoing"). The continuous external clock is also generated by the software. A LabVIEW program for a cortical recording application was written by Dr. Ying Yao and Dr. Gayatri E. Perlin. Mr. Neil K. Dhingra began modifying it for the present system. The VI is connected to the transceiver through a National Instruments Data Acquisition (DAQ) Input/Output (I/O) Card (PXI–6534 high–speed digital I/O). The transceiver manages the forward and reverse telemetry.

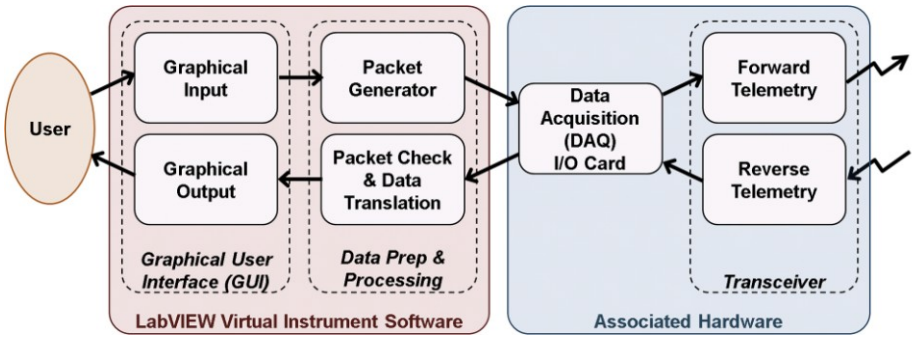



Fig. A.16: Block diagram of the external operating system.

### A.3.1.2 Graphical User Interface

The graphical user interface employs a series of tabbed screens in which the user sets the desired functions and parameters for system operation and receives visual feedback based both on the user input and on the output from the implantable microsystem, that is, graphs of the recorded neural data and testing related information. For recording, the VI should enable the user to identify recording site groups, set the pre-conditioning parameters, choose the recording mode and set the corresponding mode parameters, namely the spike polarity option, threshold value, and threshold offset for Scan Mode and the channel address for Monitor Mode. For applied waveform commands, the program facilitates the user in constructing multichannel stimulus waveforms and associated timing as well as in the corresponding parameter settings of site selection, current amplitude and polarity, and bias voltage value.

### A.3.1.3 External Data Preparation and Processing

The format of the data packets enables asynchronous wireless transmission with error checking through the use of start pulses and parity bits.

The full twenty-seven bit, forward command consists of a three-bit active-high synchronization pulse followed by a one-bit active-high strobe and the twenty bits of command/data interleaved with three parity bits as shown in Fig. A.17.

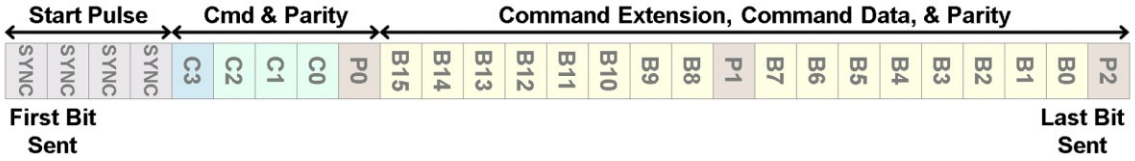



Fig. A.17: Structure of the forward telemetry path packets (incoming to the implantable system).

After receiving user input, the LabVIEW program forms the command words and adds the parity bits and start pulse to form the data packets. Even parity is used; P0 is the parity bit for C0-C3, P1 for B8-B15, and P2 for B0-B7. These packets are synchronized with the externally generated clock and sent to the transceiver with the appropriate timing.

Reverse telemetry path packets are defined for Scan and Monitor Modes as illustrated in Fig. A.18. Both outgoing packets are twenty-two bits long, begin with a four-bit active-high start pulse, and have two parity bits, P0 and P1. The parity bits are each associated with the preceding eight bits of data. As with the forward commands, even parity is used. For Scan Mode, each packet contains space for the address of four active neural channels (samples a-d), one within each of the four spike detection modules (SD Ad). The LSB for each sample is sent first. The fourth bit sent with each sample is a validity bit; when high, the sample address signifies a channel on which a neural spike was detected. The Monitor Mode packet contains two eight-bit neural signal samples (sample 0 and sample 1). Sample 0 comes first in time.

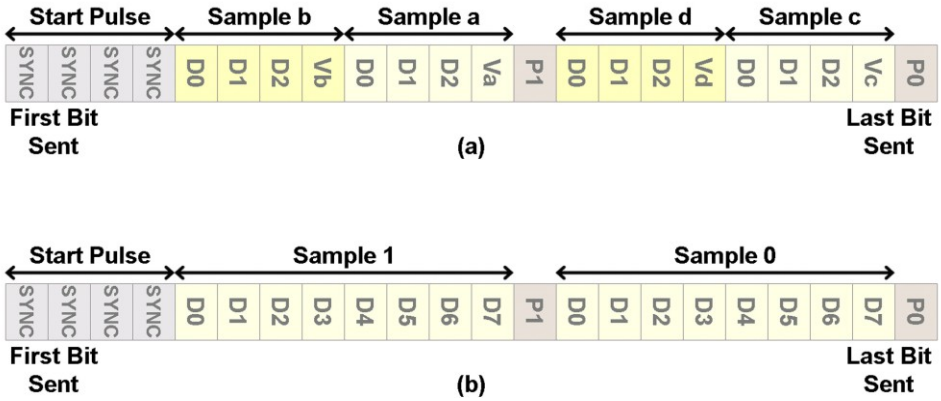



Fig. A.18: Reverse telemetry path (outgoing) packet bit definition for (a) Scan Mode and (b) Monitor Mode.

The internal transmitter sends thirty-two bit blocks; the length difference between the data packets and transmitter blocks is made up with zero bits. The LabVIEW program identifies the reception of a data packet by identifying the ten leading zeros followed by the four-bit start pulse. When the software receives a reverse packet from the transceiver, it first ensures that it passes the parity check. Then the data bits are extracted from the packet. In Scan Mode the data represents the channel addresses at which neural spikes occurred. The program translates the received information into the thirty-two channel Scan Mode plots to indicate the channel and timing of the detected neural spikes. In Monitor Mode, the data conveyed is the eight-bit amplitude of the selected channel which is extracted and graphed for user viewing. In both modes, the data is also stored for further reference and processing.

### A.3.1.4 External Transceiver

The external transceiver is composed of the transmitter for the forward telemetry path and the receiver for the reverse path as diagramed in Fig. A.19. The two units function independently.

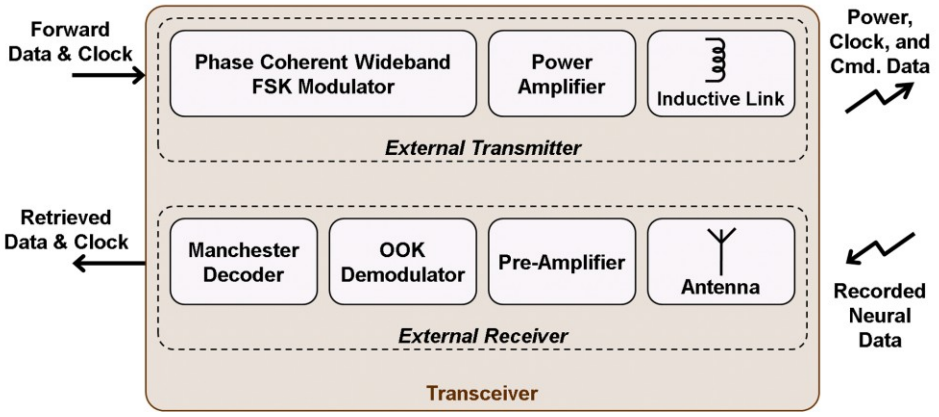



Fig. A.19: Block diagram of the external transceiver.

The data packet and clock are sent by the LabVIEW program to the external transmitter. In preparation for the wireless transmission, the signal is modulated using phase coherent wideband Frequency-Shift Keying (FSK) and then amplified. The inductive telemetry link is made with two facing E-shaped coils, one external and the other part of the implantable system. Mr. Jeffrey A. Gregory worked on the testing and construction of the transmitter-receiver unit as an individual module for use in a wireless cortical recording project.

The reverse telemetry path combines the data packets and clock signal into one through Manchester encoding and transmits with On-Off Keying (OOK) modulation and an implantable LC resonator. The outgoing data from the implantable system is received by the external antenna and pre-amplified. It is then demodulated and decoded in order to extract the data and clock which are subsequently sent to the LabVIEW program for data processing. Dr. Ying Yao developed the printed circuit board (PCB) version of the external receiver.

## A.3.2 Implantable Microsystem Fabrication Technology

The portion of the system designed for internal use includes circuitry and MEMS structures. The circuitry is fabricated as hybrid ASIC chips through the MOSIS service.

The MEMS structures take advantage of the Michigan passive probe technology which employs boron etch-stops to enable thin (approximately 12μm) devices to be created. While this fabrication methodology is not currently compatible with commercial foundry processes, past research at the University of Michigan has shown that it is feasible to create integrated CMOS circuitry with the MEMS structures to form active Michigan probes. In spite of developments in the Michigan processing technology in recent years, CMOS circuitry fabricated on-site is typically implemented in a 3μm p-sub n-epi p-well 2P/1M technology and the yield of active devices remains below 80% [63]. The device size, yield constraints, and processing time decrease the viability of implementing integrated circuitry as the Michigan fabrication technology currently stands. However, active probes have significant advantages over a hybrid structure; circuit blocks may be distributed among probes and signal multiplexing implemented, thus decreasing interconnect lead count, which is a major issue in non-multiplexed implementations. In the future, with improvements in circuit and MEMS processing capabilities, an integrated approach would appear to be the preferred solution. Nevertheless, with the present technology, the hybrid methodology offers the considerable circuit benefits of small size and increased reliability. Therefore, this approach using externally fabricated circuitry and internally processed passive MEMS structures has been selected for the bidirectional neural interface system.

## A.4 Implantable System Organization

The system has been arranged into major circuit functions; these functions are forward and reverse telemetry, control, signal processing, recording signal amplification, and stimulation current generation. Several factors influence the design and placement of these functional units:

- Small size is essential for neural applications. The dimensions of the electrode array platform are most critical in order not to obscure the view of the tissue surface during surgical implantation.
- The array should maintain its location relative to the neural tissue to sustain accurate mapping data. If feasible, forces which may cause it to move should be alleviated in order to prevent both change in relative position and tissue damage.
- The telemetry module must be located close enough to the skin to allow for reliable signal reception and transmission.

- The amplification of neural signals is advantageous to prevent distortion and loss due to noise and signal coupling. This amplification should take place as close to the electrode sites as possible.
- In order to permit biphasic stimulus currents, dual power supplies are needed for the current generators. The current sources should be located as near to the electrode sites as feasible.

Even though a foundry CMOS process is used, the combined circuitry takes significant area. Due to the design constraints, the placement of each block becomes an important engineering decision. In order to best meet the need for high signal quality, to maintain low power and small size, and to address the other design factors, two separate locations for implanted circuitry, termed circuit outposts, have been established at which reside three circuit chips. The next section presents the manner in which the internal system is situated during implantation and outlines the way the functional blocks have been organized among the circuit chips. The following sections present further detail on the individual integrated circuits.

### A.4.1 Physical Arrangement of the Implantable Microsystem

The implantable portion of the system includes two silicon platforms with a connecting ribbon cable and the front-end electrode array as illustrated in Fig. A.20. The MEMS components provide the physical structure of the implantable system. The hybrid chips are incorporated on the silicon platforms, which function as the circuit outposts, and the electrical connections are ultrasonically bonded. The front-end array contains the electrode sites used to record from and to stimulate the neural tissue. The processing of the MEMS devices was done at the University of Michigan Lurie Nanofabrication Facility (LNF) by Dr. Onnop Srivannavit and Mrs. Ning Gulari.

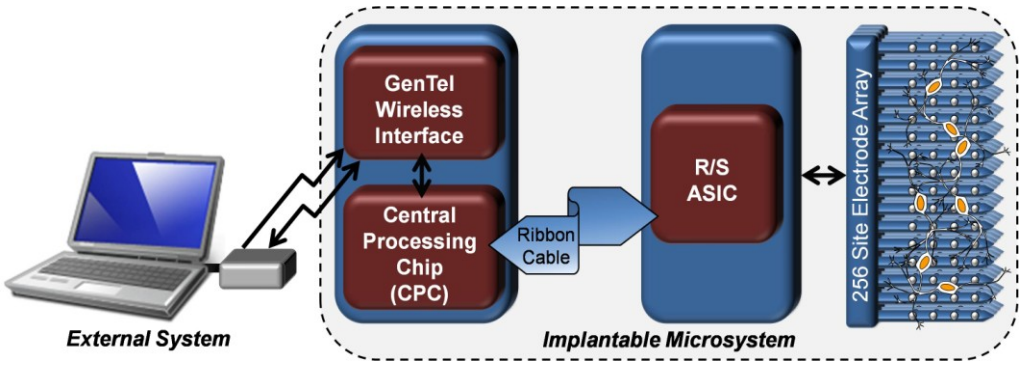



Fig. A.20: Block diagram of the complete bidirectional neural interface system [142].

A conceptual drawing of the system placement after surgery is illustrated in Fig. A.21. To prepare for implantation, the *dura mater* in the locality of interest is removed and the array is inserted through the *pia mater* and into the neural tissue. One circuit outpost is situated adjacent to the top of the array. When used in a chronic cortical application, the other circuit outpost rests between the skull and the skin. The ribbon cable forms the conduit for the electrical connections between the two outposts and allows the array to preserve its position corresponding to the neural tissue rather than being tethered to the skull.

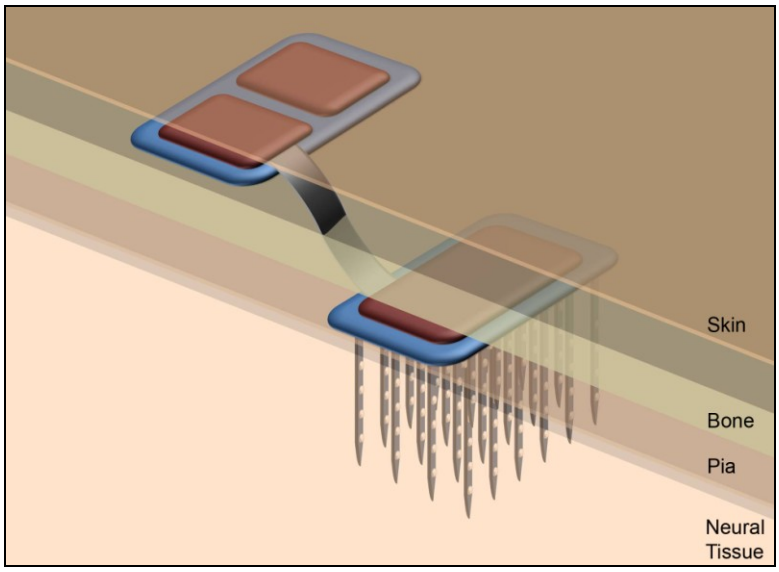



Fig. A.21: Conceptual arrangement of the implantable microsystem.

Although the ribbon cable offers the advantages of a flexible interconnect, it may also cause loss of signal integrity and it is preferred to avoid driving large amounts of power through it. The combination of design constraints referred to above led to the partitioning of the circuit blocks as shown in Fig. A.22. The circuit outpost directly below the skin stations the Generic Telemetry Module (GenTel) and associated off-chip components, which perform the bidirectional wireless communication, and the Central Processing Chip (CPC), which houses the principal control circuitry and signal processing blocks. The recording amplifiers, stimulation current generators, and the control circuitry required for these functions are located on the R/S ASIC which is placed on the circuit outpost proximate to the array.

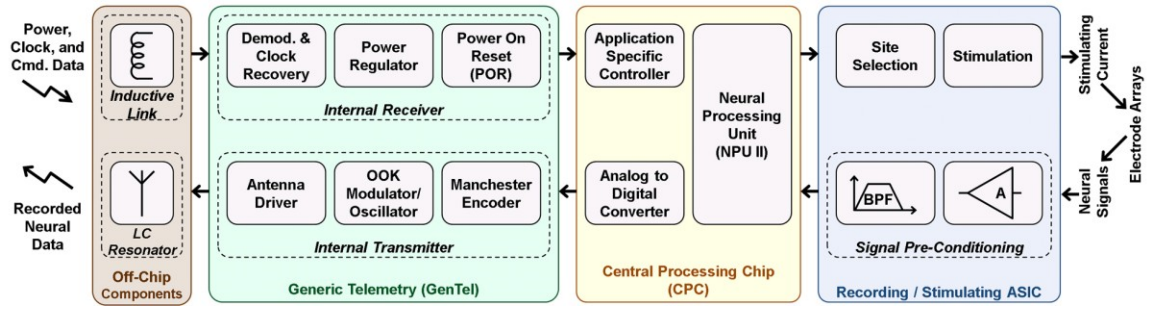



Fig. A.22: Block diagram of the functional organization for the implantable system.

### A.4.2 Generic Telemetry Module (GenTel)

For transcutaneous communication, the Generic Telemetry module (GenTel), designed by Dr. Amir M. Sodagar, is employed [143, 144]. This chip was developed as a truly "generic" wireless transmission unit, not tied to a specific application. The GenTel is fabricated through the MOSIS service in the AMI 1.5µm process.

The FSK modulated clock and control/data signal is sent through the forward telemetry path to the implantable circuitry where the inductive signal is received by the second half of a matching E-shaped coil. The E coil is one of the off-chip components on the implantable circuit platform. The signal is demodulated by the GenTel to recover the clock for synchronous communication within the implanted circuitry and to recover the data packet. The clock and data packet are sent to the Central Processing Chip. The continuous reception of command and clock signal (or the clock alone when no commands are sent) enables the GenTel to generate a regulated power supply of 3V and ground for use by all of the implantable circuitry.

For the reverse telemetry path, the Central Processing Chip sends the GenTel the prepared data packets. The GenTel uses Manchester encoding to combine the clock and data packets into one signal and digital On-Off Keying (OOK) to modulate the signal. An off-chip LC resonator is driven to wirelessly send the signal to the external receiver.

The GenTel is placed directly beneath the skin to decrease the distance for the wireless transmission. The separation of the telemetry circuitry from the front-end is also advantageous to decrease interference it may cause. A photograph of the GenTel is shown in Fig. A.23.

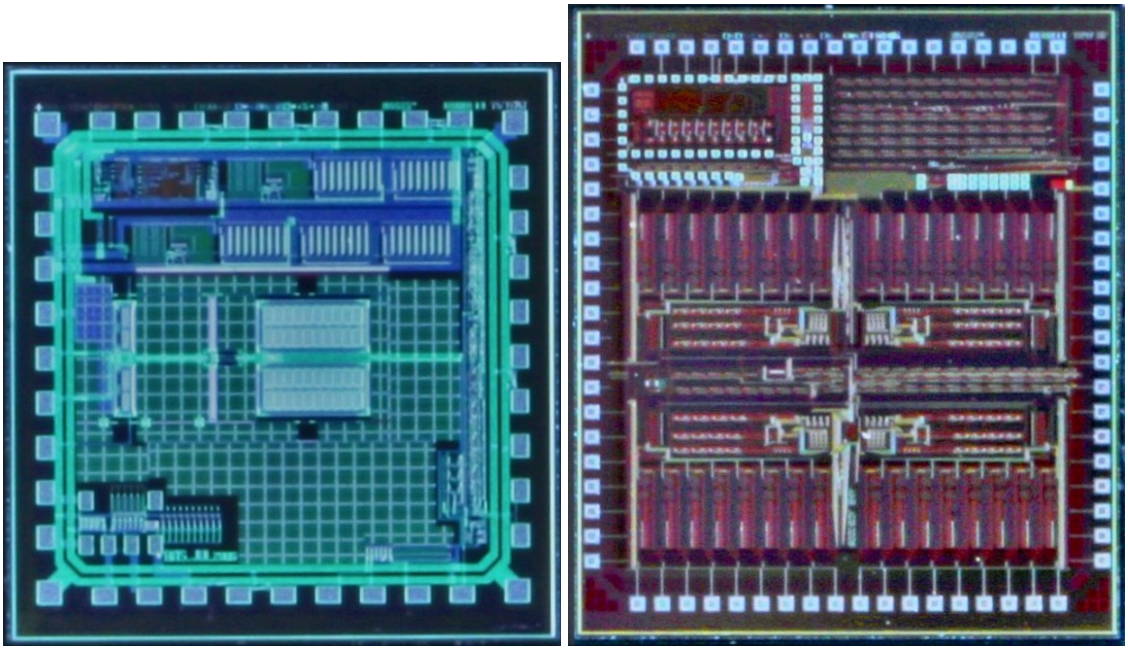


Fig. A.23: Photographs the fabricated GenTel and CPC chips designed by A. Sodagar (the two photographs are not at the same scale).

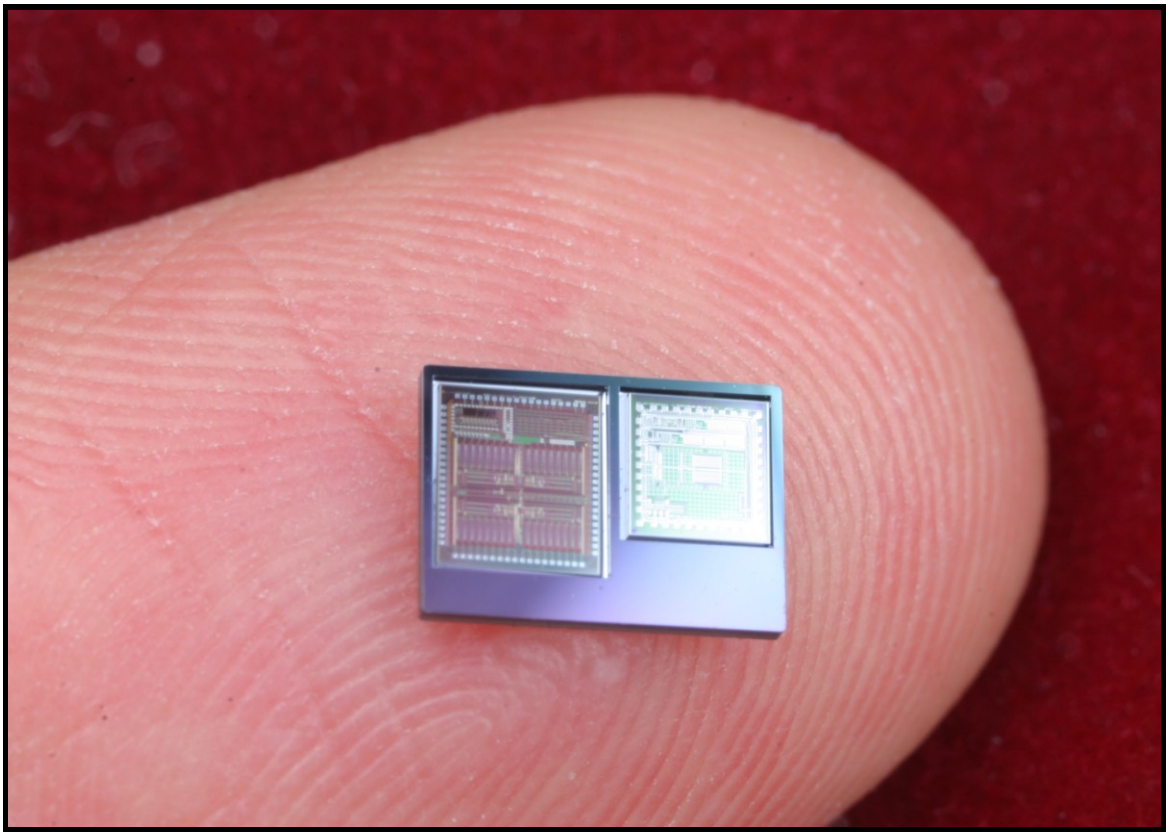


Fig. A.24: Photograph of a silicon platform with GenTel and CPC chips on a fingertip.

### A.4.3 Central Processing Chip (CPC)

The Central Processing Chip (CPC) is the second of the three circuit chips that support the implantable system functionality. This unit was designed by Dr. Amir M. Sodagar and is composed of three main blocks: the controller, the analog-to-digital converter (ADC), and the Neural Processing Unit (NPU-II). The CPC is fabricated as an ASIC through the MOSIS service in the AMI 0.5μm process. The following sections give a basic overview of the controller and the NPU-II. For further details on the CPC, please refer to [138]. A photograph of the CPC is shown in Fig. A.23 and Fig. A.24 shows both the GenTel and the CPC in a silicon platform.

#### A.4.3.1 Controller

Data packets from the GenTel are routed to the CPC controller; the structure of the incoming packets is shown in Fig. A.17. The synchronization pulse is recognized, permitting the remaining bits to be loaded into the command shift register. Error checking is performed; if the parity test is not passed, then the command is ignored. If parity check is passed, the strobe bit signals for the command to be latched. In that case, the command operational code and command data are extracted from the data packet; the resulting command word is defined as illustrated in Fig. A.1. Commands used by the CPC are decoded further.

The controller is also in charge of passing the appropriate command words to the Recording/Stimulating ASIC. Commands which have bit C3 set to one are sent to the R/S ASIC after adding a leading one as a strobe bit. Commands which have bit C3 set to zero are used by the CPC and not directly sent on to the R/S ASIC as command words. However, the system reset (RST) and appropriate power management (PWR) commands are sent to the R/S ASIC as flag lines.

#### A.4.3.2 Neural Processing Unit (NPU-II)

The Neural Processing Unit (NPU-II) processes the thirty-two channels of pre-conditioned analog neural signals from the R/S ASIC according to the selected recording mode. In Scan Mode, the NPU-II performs spike detection on the channels and marks the channels which have neural spikes. The corresponding channel addresses are packaged into data packets with appropriate leading bits and parity bits. In Monitor

Mode, the waveform from one selected channel is digitized to eight bits and this amplitude information is formatted into data packets. The data packets are sent to the GenTel for wireless transmission to the external system. The structure of the outgoing packets is shown in Fig. A.18.

### A.4.4 Recording/Stimulating ASIC

The Recording/Stimulating ASIC integrates the circuitry for site selection, pre-conditioning of the recorded neural signals, and stimulus waveform generation as well as additional functionality. This chip is located on the circuit outpost neighboring the electrode array so that the recorded signals are buffered before they are sent across the ribbon cable and so the applied waveform generation occurs in close proximity to the array. The R/S ASIC would be fabricated through the MOSIS service.

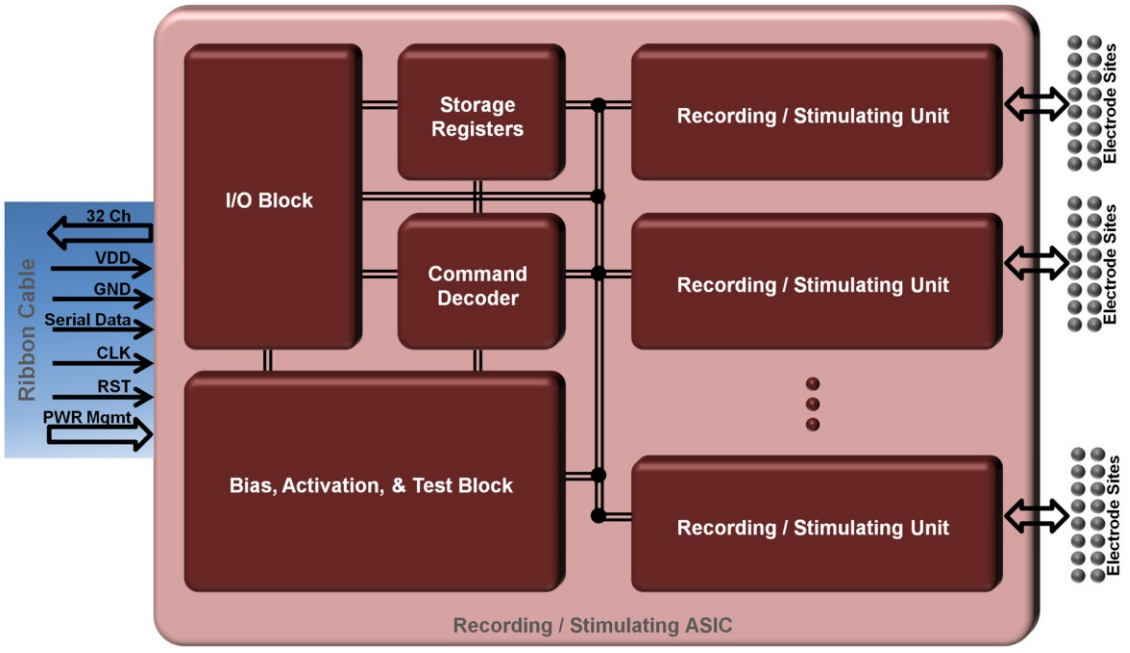



Fig. A.25: Block diagram of the R/S ASIC platform circuitry.

The block diagram of the R/S ASIC is illustrated in Fig. A.25. It subdivided into functional modules including the input/output (I/O) block, command decoder, storage registers, recording/stimulating units, and other blocks. The ribbon cable carries the forward signals from the other circuit outpost to this chip including power (±1.5V), ground, clock, serial command/data input, reset, and power management lines. Thirty-

two additional lines bring the pre-conditioned neural signals back to the CPC. In order to decrease the ribbon cable width, a time-division multiplexed option for the outgoing lines is also considered as an alternative.

The command word structure for the R/S ASIC is shown in Fig. A.26. The CPC formats incoming command words for the R/S ASIC by adding a leading active-high strobe signal. When the strobe is fully loaded in the input shift register of the controller, the command is latched and then decoded. Appropriate parameters are stored and the command is implemented.

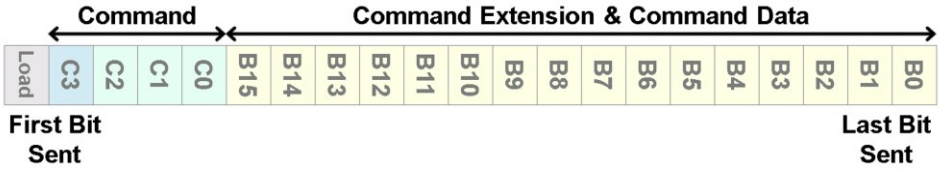



Fig. A.26: Command word structure for the R/S ASIC.

### A.4.4.2 Recording/Stimulating Unit

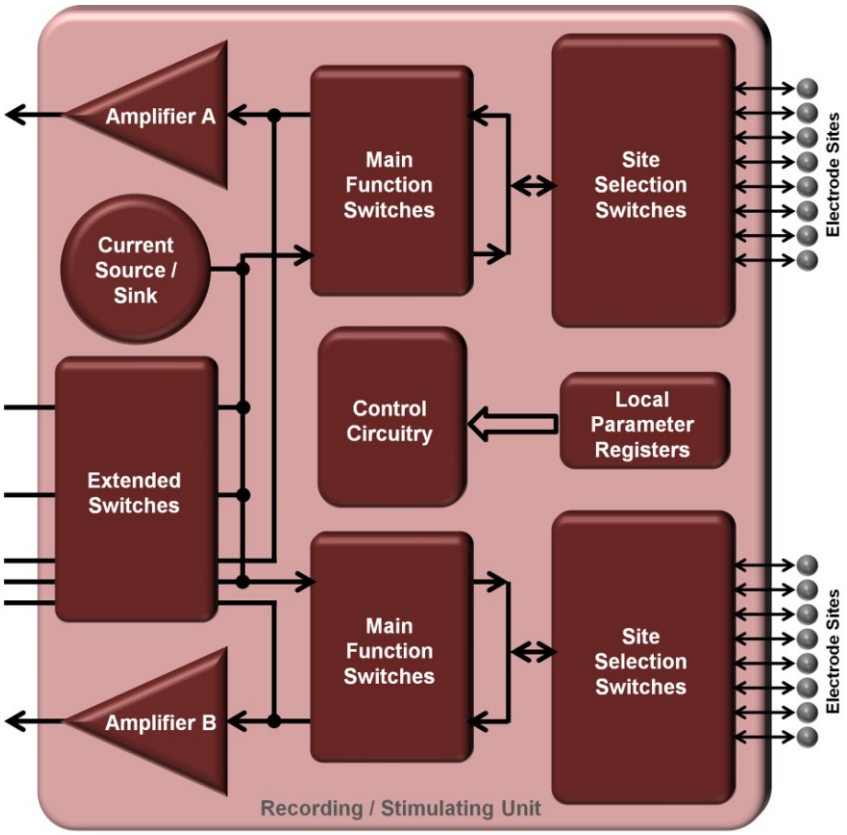



Fig. A.27: Block diagram of the Recording/Stimulating Unit. There are sixteen of these units incorporated in the R/S ASIC.

The core module for site selection, pre-conditioning of the recorded neural signals, and applied waveform generation is the R/S Unit. The R/S ASIC houses sixteen R/S Units each of which are mapped to sixteen sites on the electrode array so that a total of 256 sites are achieved. The block diagram for the R/S Unit is drawn in Fig. A.27. Each unit includes two recording amplifiers and one current source. Each amplifier may be connected to any one of eight sites; each current source may be connected to any one of sixteen sites. Thus, the collection of sixteen R/S Units supports the system's thirty-two recording channels and sixteen stimulation channels. Additional details on the R/S ASIC are elaborated in the following appendix.

### A.4.5 System Modularization

This work has been designed in a modular fashion so that one may use:

- the electrode array as a stand-alone unit (with a limited number of bonded leads),
- a simplified system consisting of a LabVIEW interface, the R/S ASIC, and the array, or
- the complete wireless system, described above.

Neuroscience laboratories may already be equipped with a set of instrumentation and software for use in conjunction with passive electrode arrays. In this case, there may be simple experiments for which site selection and other system functionality is not required. For these instances, the passive array may be directly connected to the laboratory's existing setup.

With 256 electrode sites, it is desirable to have site selection circuitry located adjacent to the array, as it would be impractical to bring out a lead for every electrode site. In conjunction with this multiplexing circuitry, amplification located close to the sites is advantageous for recording. To complete the bidirectional loop, stimulation functionality is the logical supplement. However, especially during acute experiments, wireless functionality is often not required. With percutaneous connections and a software interface, the sub-system contains all the essential functions for neural mapping experiments and other neural research. Thus, the use of a simplified system incorporating the R/S ASIC but without the other circuitry is a valuable enhancement over a passive array alone.

Nevertheless, as has been already discussed, the complete wireless system offers many advantages over partial or simplified systems.

## A.5 Three-Dimensional Electrode Array

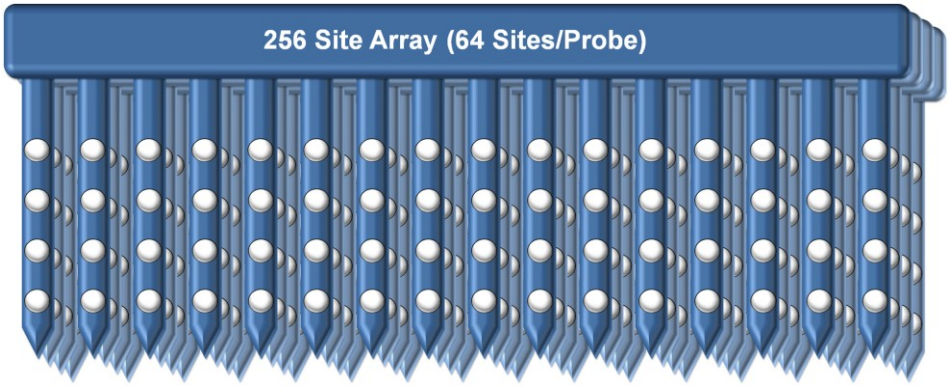
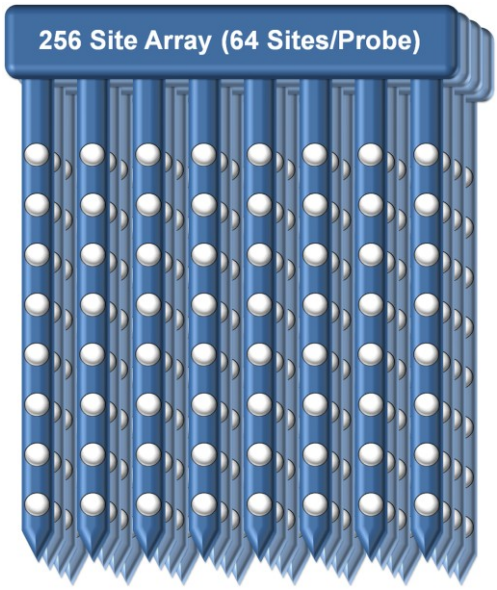
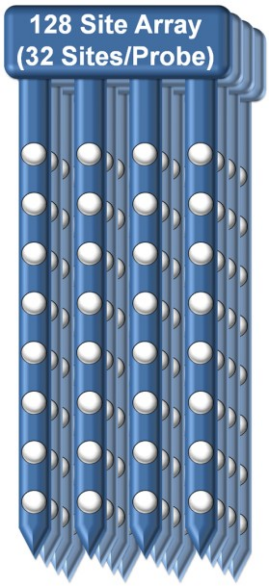
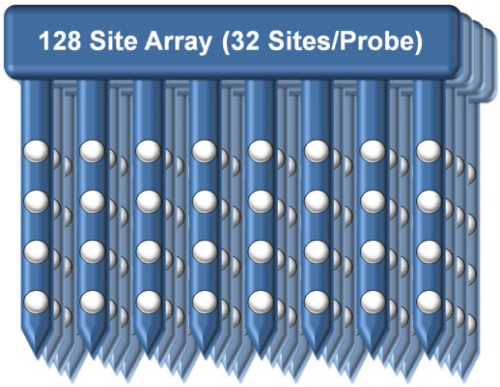
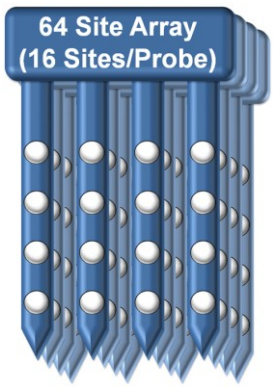
The electrode array is the principal part required for a neural interface. The arrays are batch fabricated using a boron etch-stop in a passive (without circuitry) process and then assembled individually.

### A.5.1 Electrode Array Suite

The front-end electrode array forms the basis for interfacing with the neural tissue. As such, the detailed specifications of the array vary with the particular research application for which it will be used. In order to increase the adaptability of the system, it has been designed with the possibility of modifying the array to meet individual research needs. Table A.4 shows several possible ways up to 256 sites may be configured in three-dimensions. Some of these front-end options are such that two arrays can simultaneously be used with the system. This would enable neuroscientists to implant a single system when studying the correlation between neural signals from two separate locations of the brain.

## A.6 Site Selection

With 256 electrode sites, site lead multiplexing becomes a critical issue. The mapping between current sources and amplifiers housed in particular R/S Units to the sites located on the array shanks is decisive for enabling high flexibility in multipolar stimulation and in the formation of recording site groups. This mapping becomes even more consequential during studies which employ the dual-operation of simultaneous stimulation and recording functions. For clarity and brevity, one four-probe, sixteen-shank array with four sites per shank (256 electrode sites total) has been selected to demonstrate the circuit to site connections. This scheme can be translated to probes with eight shanks and eight sites per shank by “moving” the sites on the ninth shank to the bottom of the first shank, those on the tenth to the bottom of the second, and so on. Similar multiplexing alternatives exist for other front-end arrays.

| Table A.4: Sample Arrangements of Sites on 3-D Electrode Arrays | | |
|---|---|---|
| | 16 Shanks/Probe | |
| 4 Sites /Shank |  | |
| | 8 Shanks/Probe | 4 Shanks/Probe |
| 8 Sites /Shank |  |  |
| 4 Sites /Shank |  |  |

The following sections discuss site selection in order of increasing complexity starting with selection for cases in which only stimulation is occurring. Then instances of recording without stimulation are considered. Finally, selection during dual-functionality is elucidated. While there are many options, not all site selection patterns described below are valid at all translated locations. The LabVIEW interface program should include a check for pattern validity. With novel connection arrangement, a highly compliant, multiplexed interface has been achieved.

### A.6.1 Site Selection for Exclusive Stimulation Usage

Any number of stimulation channels up to all sixteen may be used simultaneously; to take advantage of this functionality, the researcher is enabled to use a variety of stimulation configurations. The ratio of 256 electrode sites to sixteen R/S Units reduces to sixteen sites per Unit. The sixteen R/S Units (and their corresponding current sources) are labeled from 0 to 15. For greater site selection flexibility, as described below, R/S Units 0-7 connect to sites on probes 00 and 10 whereas Units 8-15 connect to sites on probes 01 and 11.

Strategic mapping was employed in designating the connections between the R/S Units and electrode sites via multiplexing circuitry so that a large repertoire of multipolar stimulation configurations would be available on each probe. The general methodology of the connections involves an "over two, down one" pattern as detailed in Fig. A.28. Multipolar stimulation configurations available include horizontal, vertical, left diagonal, right diagonal, "x" and "plus" shapes as shown in Fig. A.29. Other configurations are also possible as any site selection which consists of unique R/S Unit numbers is valid.

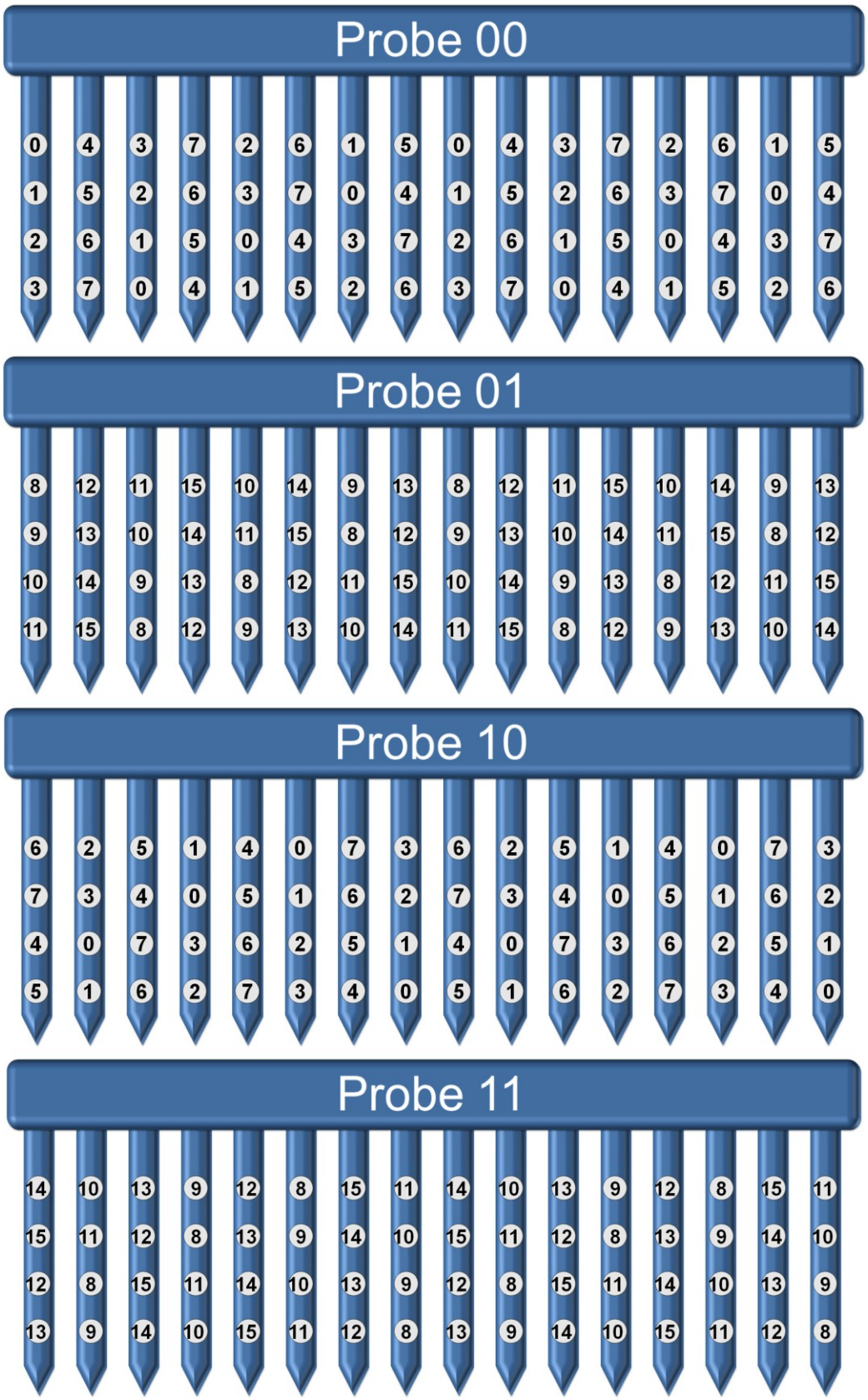



Fig. A.28: Connections between the sixteen current sources and the electrode sites.

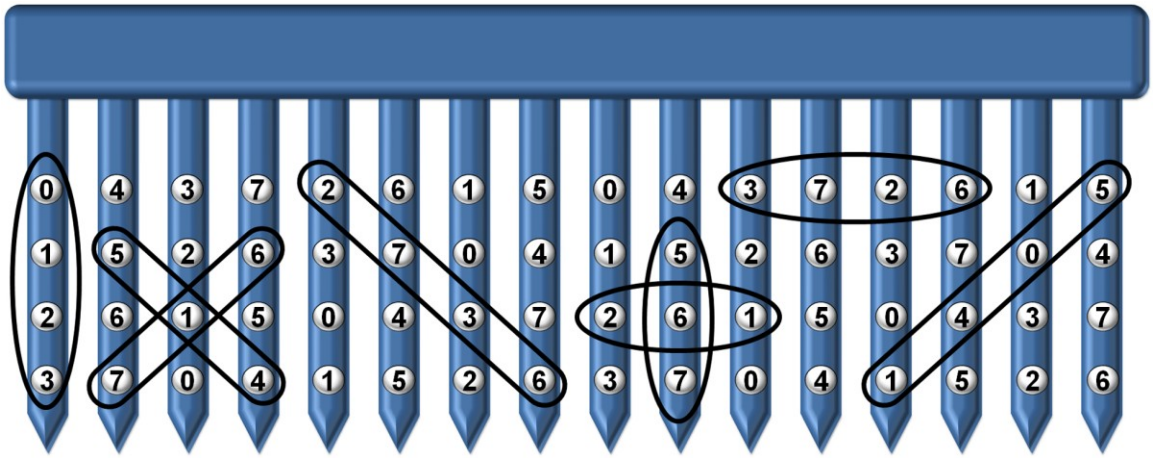


Fig. A.29: Several possible 2-D multipolar stimulation configurations.

The R/S Unit to electrode site connections were also arranged to allow multipolar stimulation configurations from probe to probe, thus profiting from the third dimension. These include horizontal patterns of straight and diagonal lines as well as horizontal "x" and "plus" shapes as illustrated in Fig. A.30. Lines which are simultaneously diagonal in both horizontal and vertical directions are also valid.

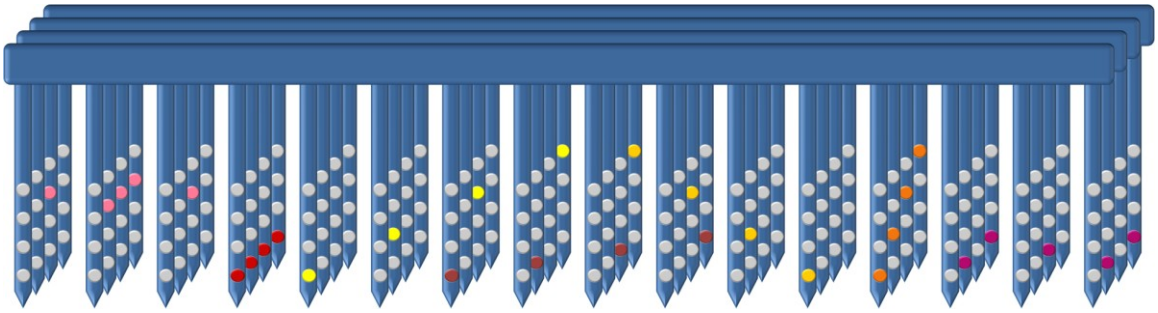


Fig. A.30: Possible 3-D multipolar stimulation configurations represented by the various colors.

### A.6.2 Site Selection for Exclusive Recording Usage

The system supports thirty-two recording channels and, as a result, a significant number of recording site groups is possible. Each recording channel has a dedicated pre-amplifier which is capable of amplifying the signal from any one of eight electrode sites. Since the sixteen R/S Units, each of which house two amplifiers, are called by unique numbers, the amplifiers are named by the corresponding Unit number plus an additional letter, "A" or "B." The connections between the electrode sites and the amplifiers are detailed in Fig. A.31.

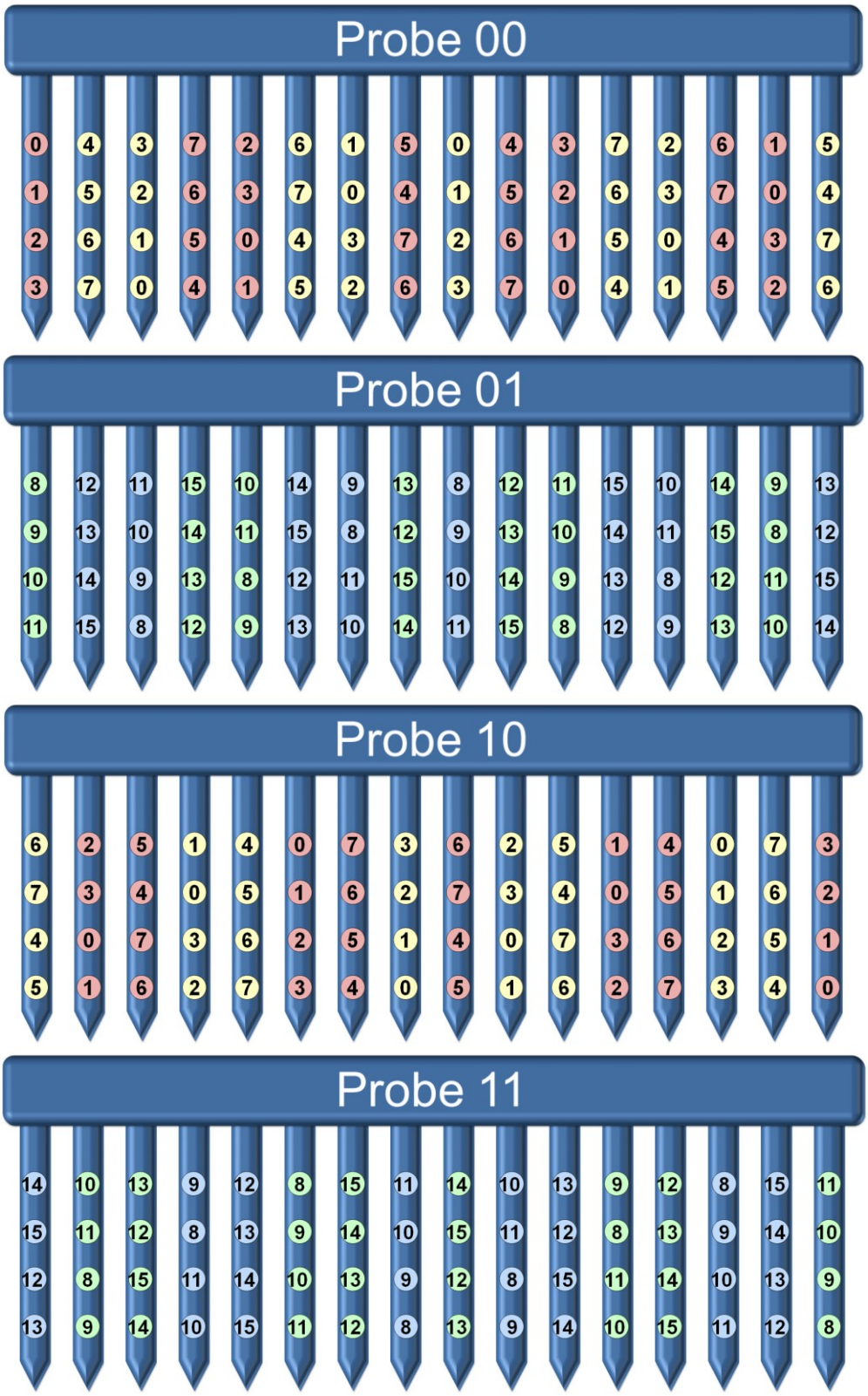



Fig. A.31: Connections between the 32 amplifiers and the electrode sites. The colors indicate one of the two amplifiers within the numbered R/S Unit: red and green signify amplifier A whereas yellow and blue signify amplifier B.

Recording capabilities on a two-dimensional probe are illustrated in Fig. A.32. Since R/S Units 0-7 are mapped to two of the probes and Units 8-15 are mapped to the other two probes, each 2-D probe can record simultaneously from up to sixteen electrode sites. Possible recording groups include: Square-4-4 (four horizontal sites by four vertical sites), Horizontal-Row-16-1 (sixteen sites in a single horizontal row), and Horizontal-Block-8-2 (two adjacent horizontal rows of eight sites each). Other options are also feasible; valid recording groups are formed with unique number/color combinations.

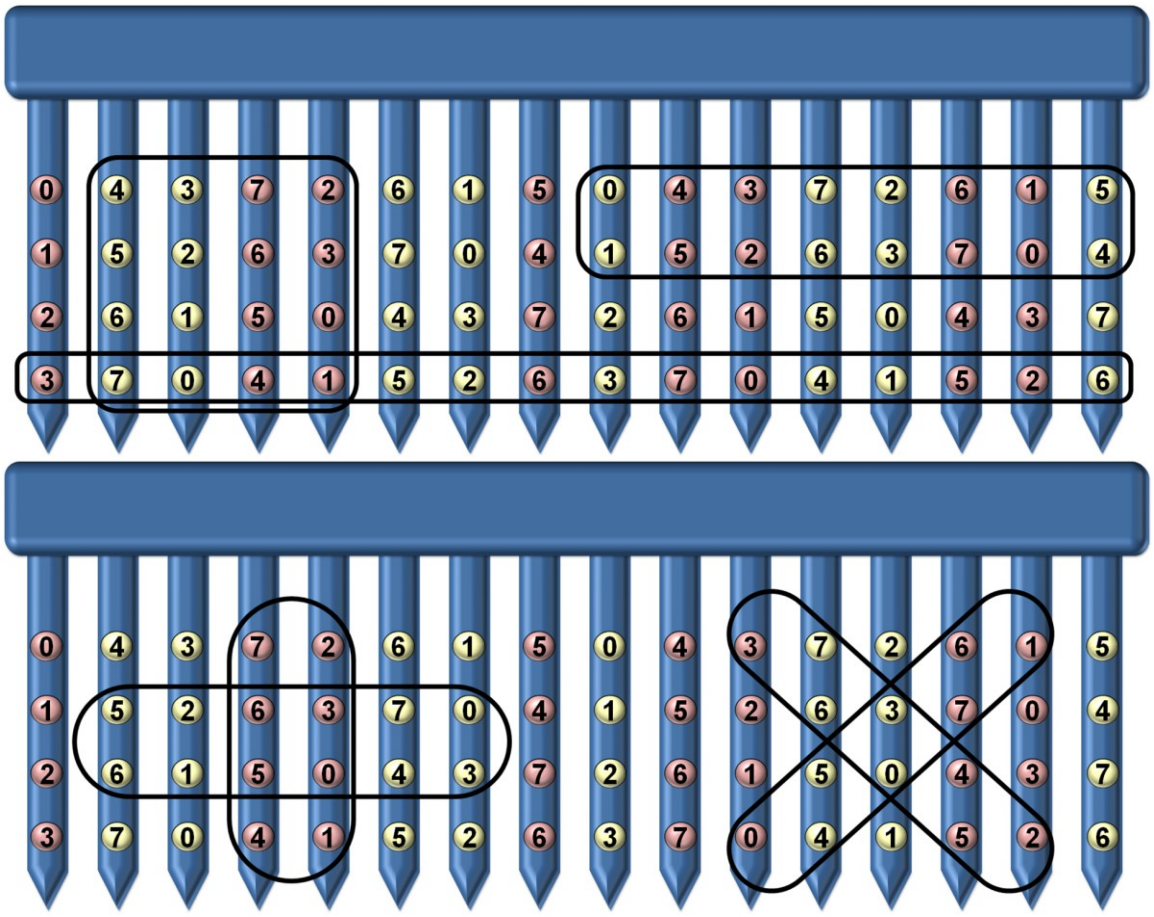


Fig. A.32: Several possible 2-D recording group configurations.

Considering the probes in parallel expands the number of simultaneous recording sites to the full 32 channels. In addition to placing the two-dimensional recording group patterns in parallel on two adjacent probes, other three-dimensional recording groups are also viable as Fig. A.33 shows.

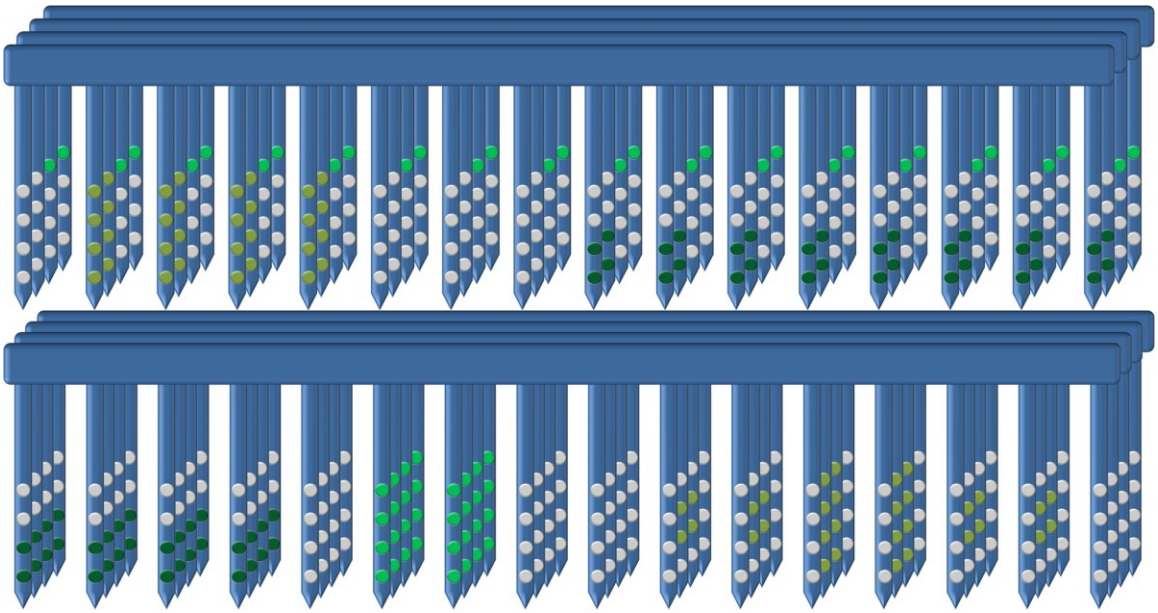


Fig. A.33: Several possible 3-D recording group configurations represented by the various shades of green.

### A.6.3 Site Selection for Bidirectional Functionality

A distinctive characteristic of this bidirectional neural interface system is the exceptionally accommodating site selection capabilities when both stimulation and recording functions are used simultaneously. This corresponds with the target application of neural mapping. Adept arrangement of the connections between circuitry and sites is indispensable for this facet of the system.

Since all electrode sites "in use" require separate channels of the total thirty-two, there are two central factors for consideration in the organization of recording and stimulation channel connections. First, in the study of multipolar stimulation patterns and current shaping, it is advantageous to have sites accessible for recording located in close proximity to those stimulating. Secondly, to provide for mapping functionality, when stimulating in one area, blocks of recording sites in remote locations should be available. In other words, the system must be able to stimulate in a primary region and to record in a secondary region such that the neurons in the first region are known or surmised to be biologically connected to neurons in the second.

Once a valid site selection has been made for stimulation, permitted recording sites are those which are identified with a number and color combination that is unique

from both the stimulation sites and from the other recording sites. For example, there are eight sites identified as "3-red" and eight as "3-yellow." If one of these sixteen sites, and more specifically, one of the eight "3-red" sites were selected for stimulation, then any one of the eight "3-yellow" sites could be chosen for recording, in addition to any one site from each of the other number/color groups, for a total of thirty-one recording sites.

To assist in the study of current shaping, the ability to record from sites near the sites selected for stimulation has been included. When performing multipolar stimulation on one probe, there are neighboring recording sites available within the same plane as shown for several configurations in Fig. A.34. Additionally, since alternating probes use stimulation and recording channels from R/S Units 0-7 and from R/S Units 8-15, in the case of multipolar stimulation on one probe, the sites in a parallel plane on an adjacent probe are available for recording as illustrated in Fig. A.35.

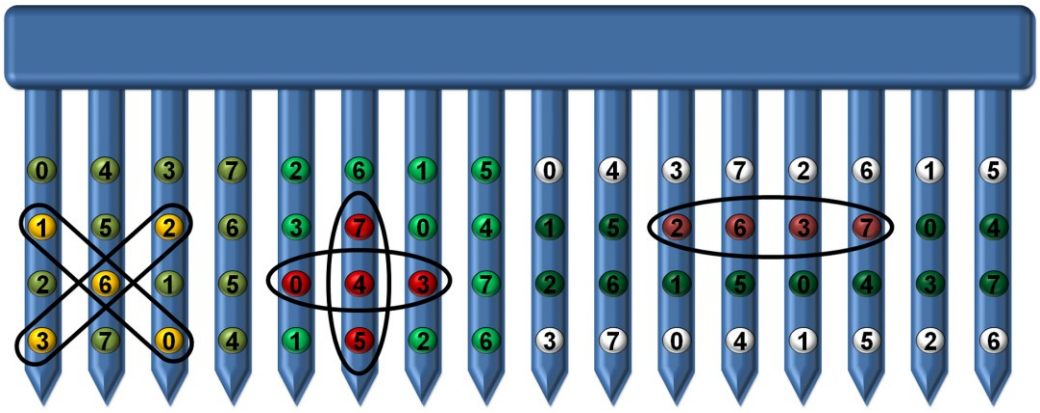


Fig. A.34: Sample configurations for in-plane recording near multipolar stimulation sites. Red and yellow indicates stimulation sites while shades of green signify recording sites.

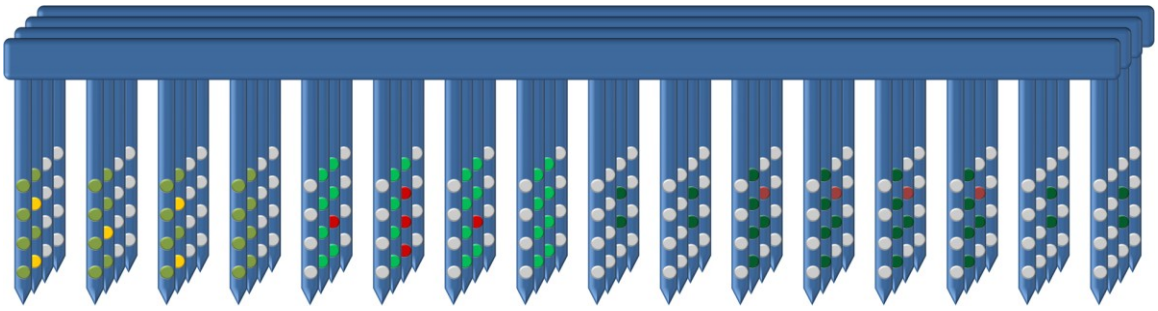


Fig. A.35: Sample configurations for in-plane recording near multipolar stimulation sites and additional recording in a plane parallel to the stimulation sites. Red and yellow indicates stimulation sites while shades of green signify recording sites.

Mapping functionality requires stimulation and recording in separate regions. Such capability is presented in Fig. A.36.

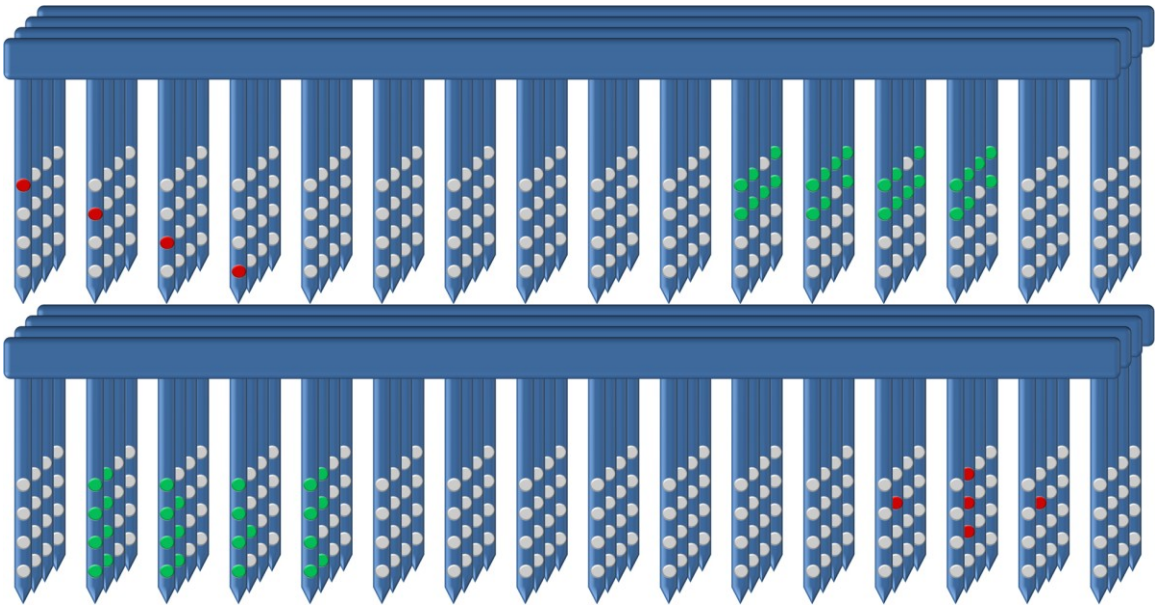


Fig. A.36: Examples of 3-D bidirectional functionality. Red indicates sites selected for stimulation while green signifies sites chosen for recording.

### A.6.4 The Use of LabVIEW in Site Selection

As discussed above, the circuitry is constructed to enable high flexibility in the designation of simultaneous multipolar stimulation and recording functionality. In order to provide the user with a way to easily manage the site selection, the LabVIEW VI should include a graphical interface for this purpose. Then, through the software, one may designate sites individually for their intended function or may use pre-programmed groups for a faster setup. The VI should perform validity checking to ensure only permissible selections are made.

## A.7 Conclusions

This appendix presented the overview of the envisioned system capabilities and the underlying structure to support these features. The external portion of the system includes the software and hardware required for a graphical user interface and for wireless communication with the rest of the system. The implantable portion of the bidirectional neural interface is composed of three hybrid chips, foundational MEMS structures, and the 256-site electrode array. The system circuitry, along with the full

command repertoire, enables thirty-two recording channels and sixteen stimulation channels, with extensive alternatives for applied waveform generation and site selection, during operation with bidirectional functionality.

## APPENDIX B

## FRONT-END DESIGN FOR THE NEURAL INTERFACE SYSTEM

The system front-end consists of the Recording/Stimulating ASIC (R/S ASIC) and the electrode array. This appendix presents further detail on these two parts. As indicated above, the front-end chip, electrode array, and LabVIEW interface may also be used as a mini-system without the neural processor or wireless interface. The conceptually designed R/S ASIC is the front-end circuit module, designated for site selection, pre-conditioning of neural signals, and generation of stimulus waveforms. The block diagrams for this module are shown again for convenience in Fig. B.1 illustrating the relationship to the whole system. The first section looks at the general features and circuit blocks related to global functionality; the second section steps into the R/S Unit sub-block, and the third presents one instantiation of a 256-site electrode array

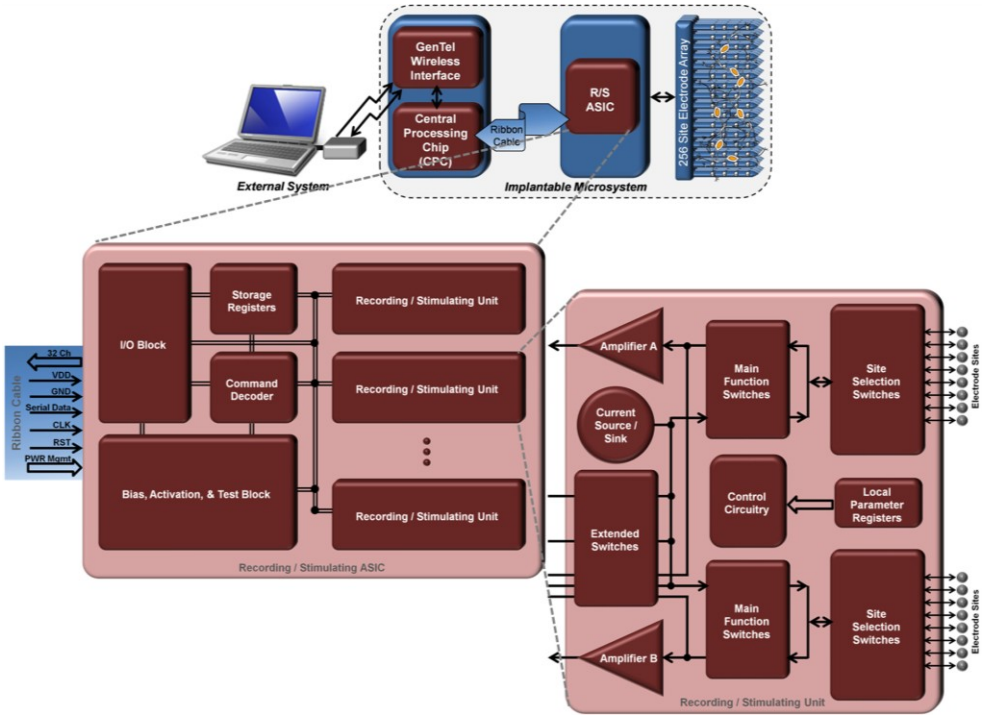



Fig. B.1: Block diagrams of the front-end Recording/Stimulating ASIC showing its main modules and place within the system. See Fig. A.25 and Fig. A.27.

## B.1 Recording/Stimulating ASIC Global Circuitry

The global circuitry of the R/S ASIC includes the input/output (I/O) block, the command decoder, the global storage registers, and the bias, activation and test block. Fig. B.2 shows the R/S ASIC blocks with the main functions included in each.

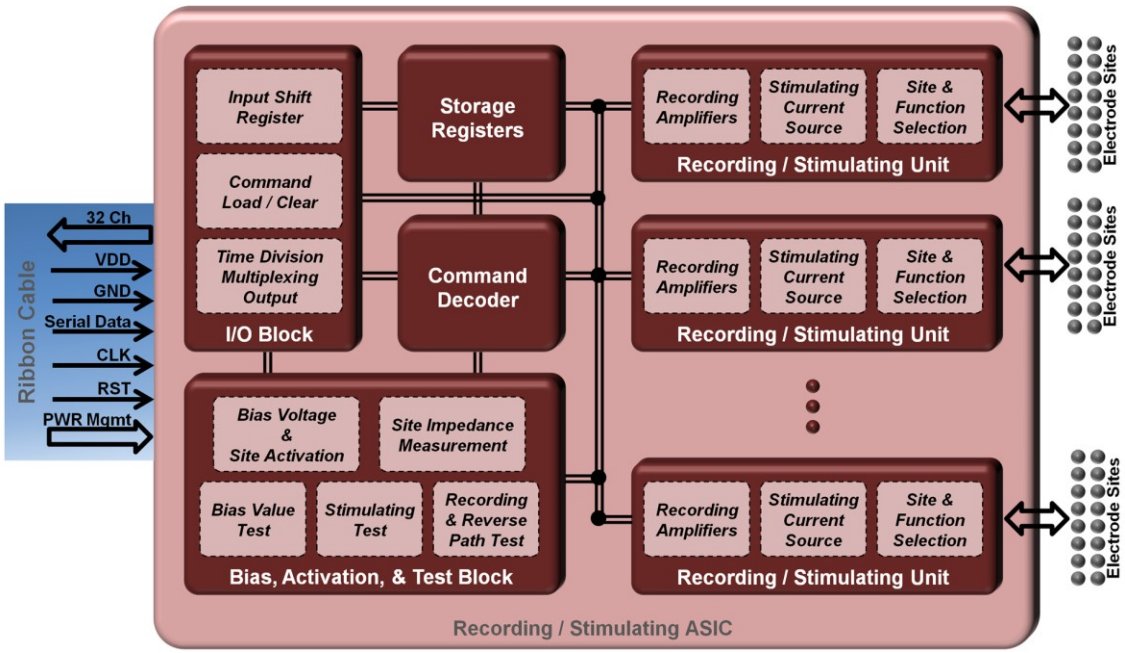



Fig. B.2: Block diagram of the R/S ASIC showing functions within the blocks.

### B.1.1 I/O Block of the R/S ASIC

Commands incoming to the R/S ASIC arrive at the input/output block. The command word structure for the R/S ASIC is presented in Fig. A.26 and Fig. B.3 illustrates the I/O block.

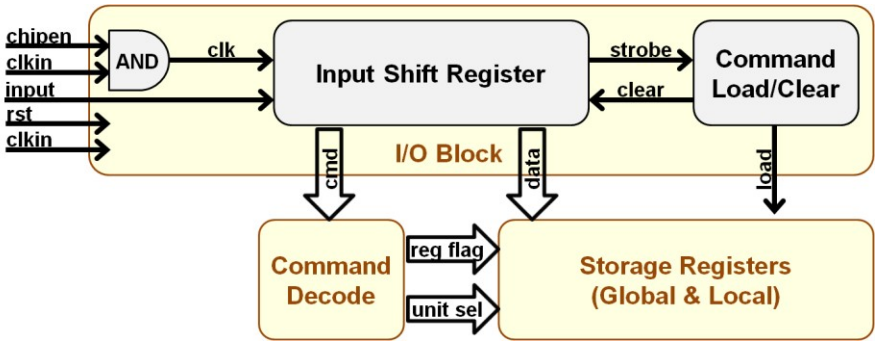



Fig. B.3: Block diagram of the I/O block and its relation to the command decode block and storage registers.

The serial incoming data is clocked into a twenty-one bit, serial-input, parallel-output shift-register. The input shift register is composed of an input D flip-flop followed by a series of twenty RS flip-flops. The arrival of the strobe bit in the farthest register generates a load signal after a small, set delay. This signal is used in conjunction with the command decoder output to load registers as appropriate. Another set delay is instantiated before the input register is cleared. This delay has been simulated to be long enough for decoding of the command and storage of the data, but short enough to permit a large clearance in preparation for the subsequent command. The delays are made using slow inverter chains as drawn in Fig. B.4.

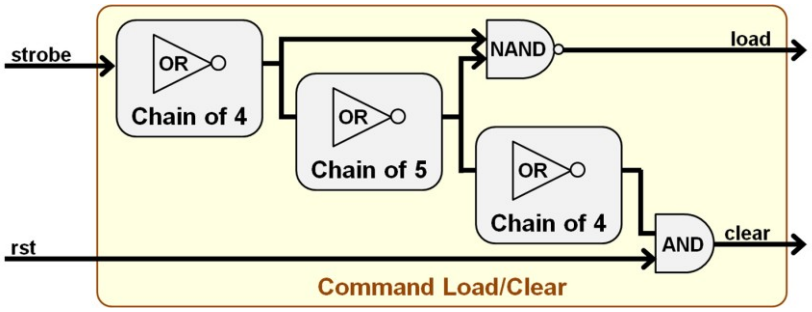



Fig. B.4: Block diagram of the register load and command clear block.

The current iteration of the Central Processing Chip (CPC) which interfaces with the R/S ASIC does not include a block to handle a time division multiplexed (TDM) format of the recorded neural signals coming from the R/S ASIC. However, it is included in the R/S ASIC diagram as a possible future enhancement to reduce the number of outgoing leads.

### B.1.2 Command Decoder

Decoding circuitry determines the command function. A simple three-to-eight binary decoder with active-low outputs is used to decode the command operational code (op-code) and to generate command flags. A four-to-sixteen bit decoder is likewise used to determine the R/S Unit address to instantiate commands intended for a specific Unit with a unit enable signal. The output of the command decoder is only valid and used when the corresponding load flags are active.

### B.1.3 Global Storage Registers

The basic functionality for most commands involves the use of parameters and flags stored in global and local (within R/S Units) registers. Fig. B.5 illustrates the global registers. These include:

- four sixteen-bit registers for the Fast Setup applied waveform command flag bits
- one four-bit register for the bias voltage value setting,
- possibly one register for globally set recording parameters such as gain, offset, and bandwidth, and
- possibly one register for testing and initialization related features.

The last two registers described are tentative pending on the final details of the system structure. Data is parallel-loaded into a given global register; the registers are composed of gated SR latches, which are therefore sensitive to the inputs whenever then enable is active. The enable is active only when the corresponding command flag and the load register flag are both active.

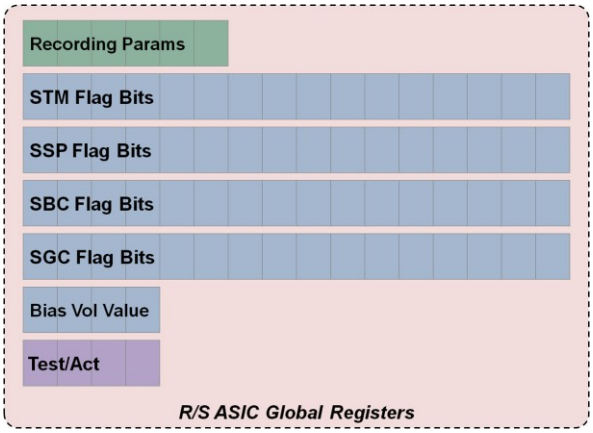



Fig. B.5: The global registers of the R/S ASIC.

### B.1.4 Bias, Activation, and Test Block

In order to achieve enhanced functionality and to instantiate testability while also minimizing area, the bias voltage generation, site activation, and test features are integrated into one global module. *In vivo* testing is an important requirement for chronically implanted systems. This system enables wireless electrode site activation as well as testing of the

- bias voltage value,
- stimulation current sources,

- array front-end and electrode impedance, and
- recording amplifiers and reverse path.

Fig. B.6 shows an overview of the bias, activation, and test block on the R/S ASIC along with one extended switches sub-module incorporated on each R/S Unit; subsequent sections detail the parts of these blocks which are used for each feature.

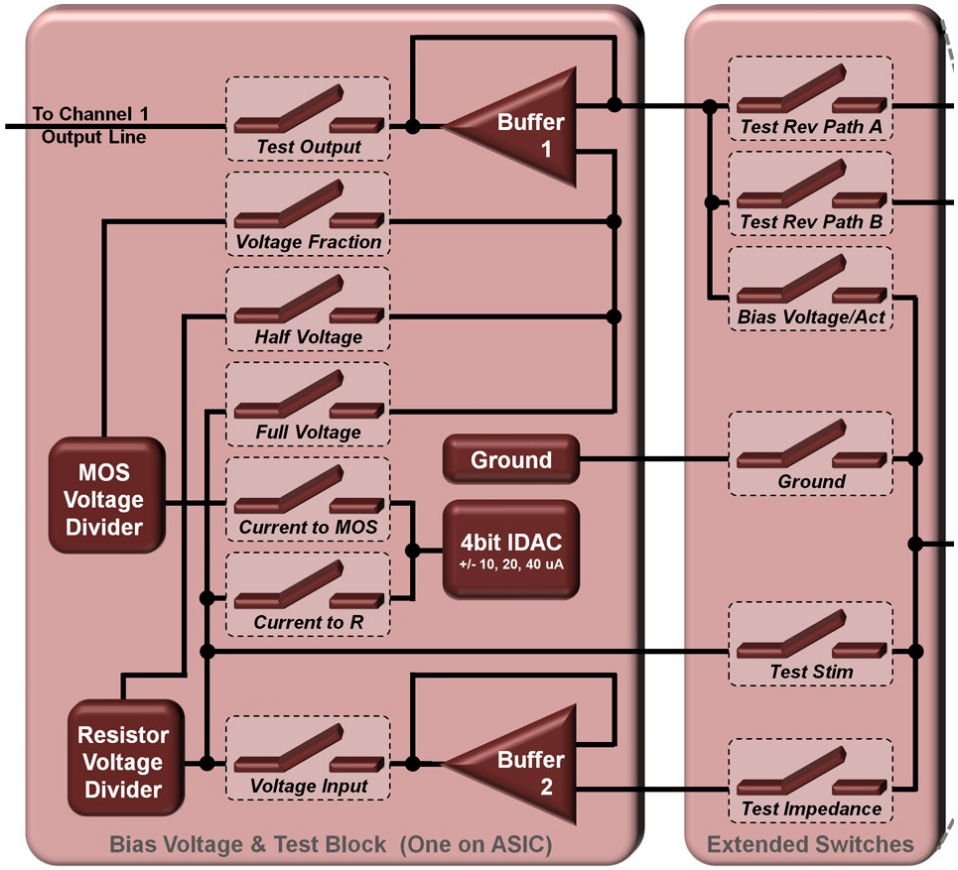



Fig. B.6: Block diagram of the global bias, activation, and test block incorporated on the R/S ASIC and connections to one extended switches sub-module which is instantiated on each R/S Unit.

### B.1.4.2 Bias Voltage Generation

When employing the neural interface system, the user has the ability to select one bias voltage value within ±0.98V and connect one or more sites to this level as Section A.2.2.1 describes. In order to implement this functionality, a voltage-output digital-to-analog converter (VDAC) is used which consists of a current output digital to analog converter (IDAC), an on-chip resistor, and a buffer as illustrated in Fig. B.7.

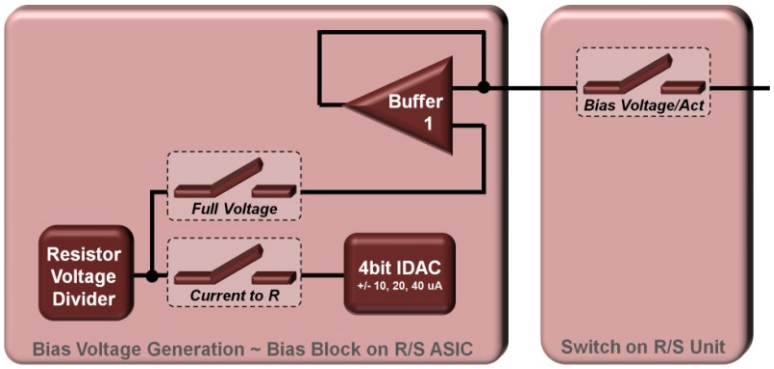



Fig. B.7: Diagram of the bias voltage generation.

The IDAC has sourcing and sinking current strands for 7μA, 14μA, and 28μA outputs. The polarity bit determines if the sourcing or sinking strand is used. Each strand is turned on or off by the respective bit in the bias voltage amplitude. The current is directed to a 20kΩ resistor and the voltage across the resistor is buffered. This enables the full ±0.98V range with 0.14V steps. In order to accommodate for large current draw when multiple sites are activated, the option of connecting multiple buffers in parallel should be considered. As a power savings technique, the reference current on the IDAC may be turned off with the corresponding power management (PWR) command bit.

For design simplicity the current to voltage conversion is envisioned as a simple, doped polysilicon resistor. While on-chip resistor values are known to vary widely from run to run, the absolute value of the resistance is not critical as the bias level options are flexible. If it is determined that resistance also varies considerably from die to die within one run, then a differential voltage design, which depends on the ratio of two resistors rather than on the absolute value of one resistor, may be preferred. Such a design would add complexity and area so should be avoided if possible. During *in vitro* testing and acute experiments the effect of ambient light on the resistance should also be taken into account. When fully implanted, light variations will not be present to cause resistance variations.

### B.1.4.3 Electrode Site Activation

The bias voltage circuitry can be employed to enable simultaneous multisite activation through the wireless commands and a squarewave voltage signal. The LabVIEW interface would allow the user to select the negative and positive voltage

levels, the activation frequency, and the number of cycles; typical settings are -0.7V to +0.7V with a 0.1V/s signal [145, 146]. Sixteen sites at a time are connected to the bias line and activation is performed. After the first group is activated, the next set of sixteen sites is connected and the procedure continues until all sites are activated.

### B.1.4.4 On-Chip Test of the Bias Voltage Value

Wireless, on-chip testing of bias voltage value requires minimal additional circuitry. The output of the amplifier which is normally connected to the channel one analog output line is disconnected and the buffered bias voltage output is connected to this line through the test output switch, as shown in Fig. B.8.

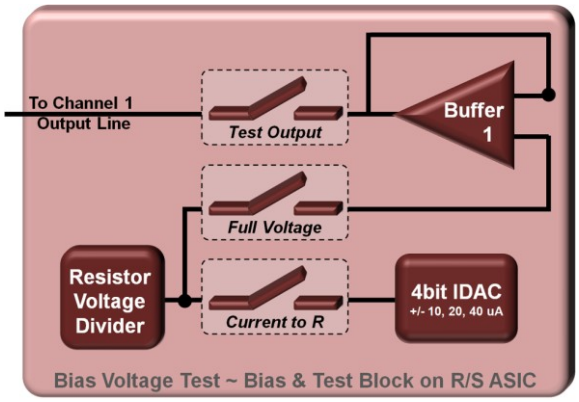



Fig. B.8: Test configuration for the bias voltage value.

### B.1.4.5 On-Chip Test of Stimulation Current Sources

The circuitry included for the bias voltage generation and test can also be used with minor modifications in order to test the functionality of the stimulation current sources. In this mode, one of the sixteen current sources is connected to the on-chip resistor in the bias, activation, and test block through the test stimulation switch in the corresponding R/S Unit as illustrated in Fig. B.9. The voltage across the resistor is buffered and sent to the channel one analog output line through the test output switch. With a current amplitude span of 1μA to 31μA and a 20kΩ resistor, the output voltage will extend from 20mV to 620mV; this is within the acceptable range of CPC input block. The exact current to voltage correspondence can be calculated once the fabricated resistance value is determined. During this test the bias voltage IDAC is disconnected from the resistor and the channel one amplifier is disconnected from the output line. The

current output determined by this test must be evaluated according to the testing methodology; in normal function the electrode array may have significantly higher impedances than the test resistor. This issue is discussed further in the section focused on the current source.

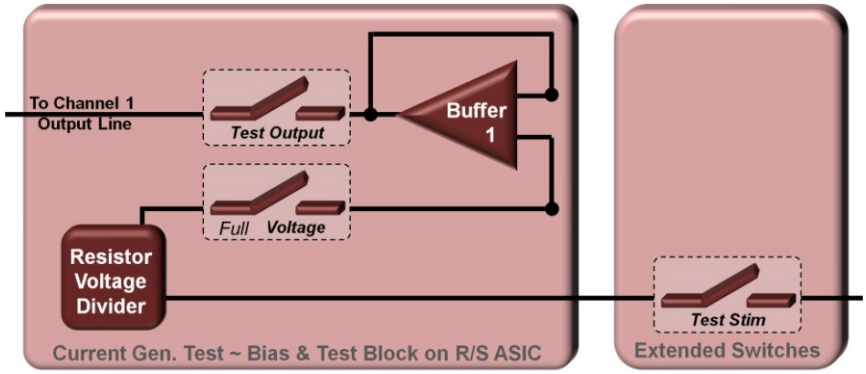



Fig. B.9: Test configuration for current source assessment.

### B.1.4.6 On-Chip Test of Electrode Impedance

In order to test the electrode impedance, a 1kHz squarewave current is generated by the stimulation current sources using the polarity (POL) command. This current is directed to the selected site and the back voltage is sent to the bias, activation, and test block through the test impedance switch as shown in Fig. B.10. The measured value is buffered, divided down, and buffered again, then sent to the channel one analog output line through the test output switch. The voltage division is performed in order for the output range to be in the acceptable input range for the CPC. The target for site impedance is less than 40kΩ including the resistance of the lead lines. In this case, the maximum back voltage would be 1.24V which would give the current source headroom for a voltage compliance of up to 0.26V with a ±1.5V supply. Lower than maximum current would then be used for the impedance test so that the maximum back voltage falls in the ±1V range of the CPC input block. However, as electrode sites that are inactivated and do not have any additional treatments may have an impedance closer to 1.5MΩ, a resistor divider is included so the back voltage can be divided down to the CPC input range. It is recognized that the maximum measurable back voltage is limited by the power supply and current source compliance. Although the pre-test value may be beyond

the measurable range, pre-testing verifies if the initial site impedance is “large” so a drop due to activation can be acknowledged after activation.

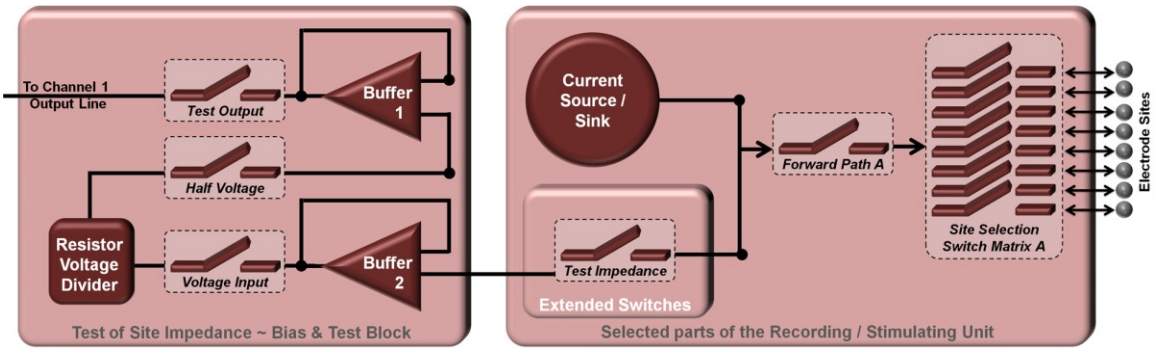



Fig. B.10: Test configuration for site impedance measurement.

### B.1.4.7 On-Chip Test of Recording Amplifiers and Reverse Path

Testing of the recording amplifiers and reverse path is crucial for distinguishing between “quiet neurons” and faulty circuitry. For a test signal, a 1kHz squarewave is generated by the current source from R/S Unit Zero and an appropriate resistor value for conversion to voltage. Two approaches are to use the amplifier with a gain of 1000, as typical in recording, or to use a gain of 100, for lower constraints during test. The basic test configuration is part of the test block shown in Fig. B.6.

Neural signals are on the order of 500μVpp in amplitude and the designed amplifier gain is 1000 [147]. In order to correspond to this input and gain, the first approach uses a signal with 1mV amplitude. To achieve this, the output of the IDAC is set to the lowest level of current (1μA) and steered with the Test Impedance switch to a MOS voltage divider in the bias, activation, and test block. A voltage tap enables a small voltage of 500μV to be buffered and sent to the input of the amplifier under test through the corresponding test reverse path switch on the R/S Unit. With the amplifier set to a gain of 1000, the output voltage should be a bandpass filtered version of a 1kHz, 0.5V squarewave.

In the second case, the output of the IDAC is set to the lowest level of current (1μA) and steered with the test impedance switch to the 20kΩ, on-chip resistor in the bias, activation, and test block. A voltage tap enables the quarter voltage (5mV) to be buffered and sent to the input of the amplifier under test through the corresponding Test Reverse Path switch on the R/S Unit. With the amplifier set to a gain of 100, the output

voltage should be a bandpass filtered version of a 1kHz, 0.5V squarewave. The advantages of this technique are that the input signal is significantly above the noise level and the output is still within the range of the CPC input. The disadvantages include that the additional circuitry to have a second gain option (of 100) on the amplifiers to keep the output within ±1V and that the gain of 1000 can only be tested *in vitro*.

## B.2 Recording/Stimulating Unit

The core functions of the R/S ASIC are performed within the sixteen Recording/Simulating Units, including site selection, pre-conditioning of the recorded neural signals, and applied waveform generation. Fig. B.11 illustrates the block diagram for the R/S Unit.

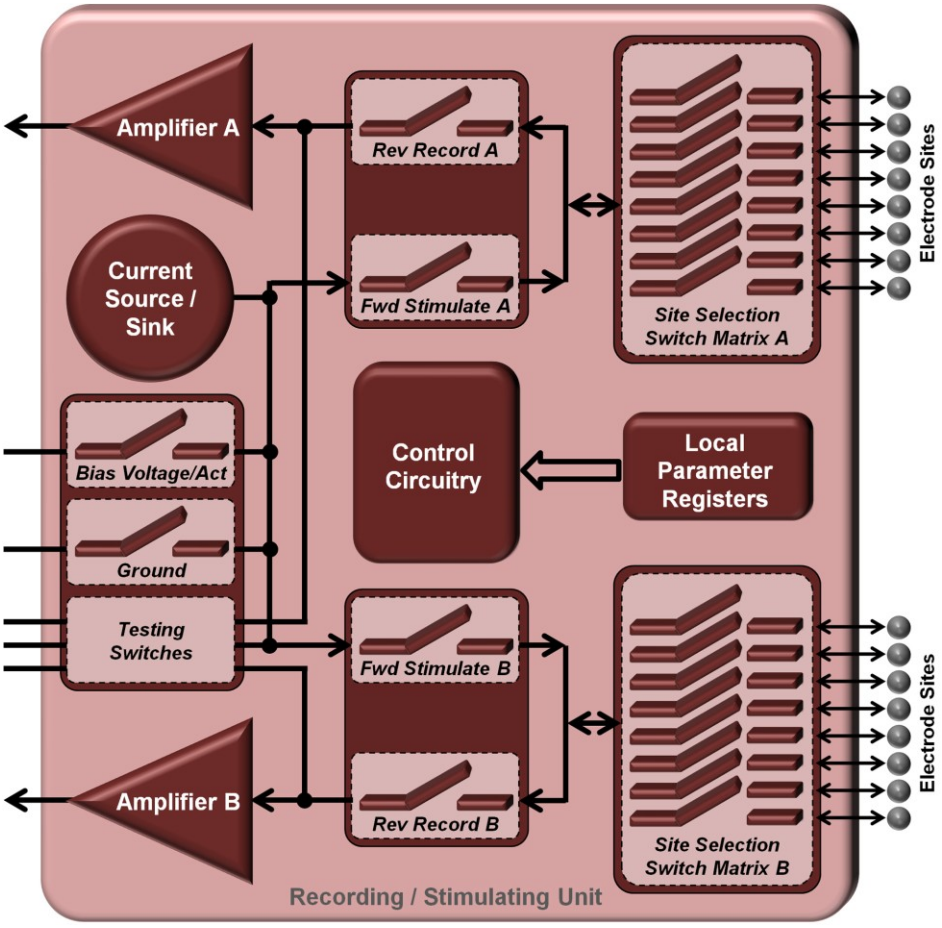



Fig. B.11: Block diagram of the Recording/Stimulating Unit. There are sixteen of these units incorporated in the R/S ASIC.

### B.2.1 R/S Unit Parameter Registers

Parameters and flags particular to the functionality of each R/S Unit are stored locally within each Unit. Fig. B.12 shows the local registers. These include:

- two three-bit registers for the recording site address, one corresponding to each amplifier,
- two registers for the recording amplifier parameters, one for each amplifier,
- one four-bit register for the stimulation site address,
- two five-bit registers for the negative and positive stimulation amplitudes, and
- one register for testing and initialization functions.

Data is parallel-loaded into a given local register (gated SR latch) when the corresponding command flag, the load register flag, and the unit address flag are all active.

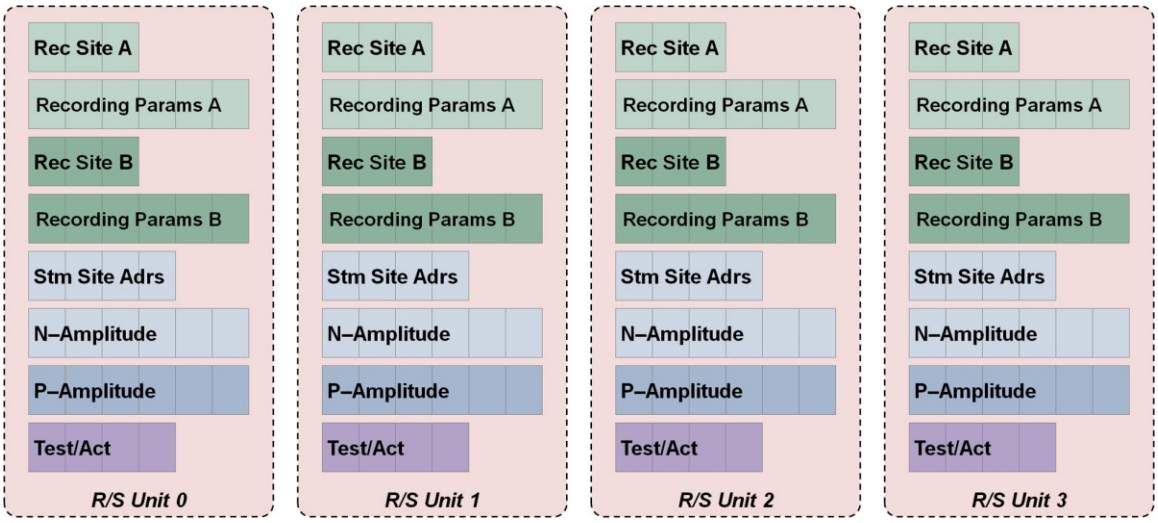



Fig. B.12: Conceptual diagram illustrating the local registers within the R/S Units. Only Units 0-3 are shown; other units have the same architecture.

### B.2.2 Site Selection

Site selection is used during normal system functionality as well as during testing. The sixteen sites corresponding to each R/S Unit are divided into two banks. Each bank of eight sites has an individual site selection switch matrix. The switch controls are based on a standard three to eight binary decoder with active-low outputs. In regular operation, the state of the stimulation status (STM) flag for the Unit and the most significant bit of the stimulation address governs whether the recording or stimulation address is used for the site selection decoding for each bank.

### B.2.3 Recording Amplifier

The recording amplifier is one of the critical blocks of the reverse path. The CPC analog input requires a single-ended signal in the range of ±1V if the 3V power supply span is centered around ground. Chapter IV details the neural recording amplifier designed for use with this system.

### B.2.4 Stimulation Current Source

The current source includes a programmable five-bit amplitude in the range of ±31μA with 1μA resolution. Several current source topologies were considered through simulation. However, due to the possibly large electrode array impedance, a current source with high voltage compliance is one of the most critical issues. Therefore, a simple current source topology is recommended.

## B.3 256-Site Electrode Array

To take full advantage of the high site count and site selection capabilities of the bidirectional interface system, a 256-site electrode array was designed. This 256-site universal array consists of four, eight shank probes, with eight electrode sites per shank. The shanks are three millimeters long and spaced with a pitch of 200μm; the sites have a pitch of 200μm and area of 177μm$^2$ or 1000μm$^2$. Electrode sites are typically considered to be able to record from neurons up to 100μm vertically away in rat cortex or hippocampus [147-149]. Thus spacing the electrodes at a 200μm pitch in all three directions covers significant neural volume within the array. When utilized in other neural structures and in the horizontal plane, the recording range may be smaller. A block platform is used for this array; Fig. B.13 shows a conceptual array sketch. As with the AVCN-DCN array, integrated flexible cables are used for signal routing. Fig. B.14 through Fig. B.17 present images of the fabricated 3-D array.

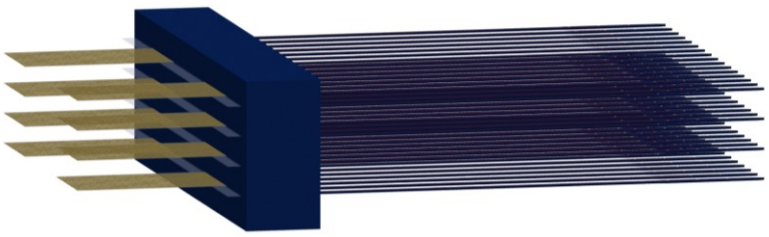
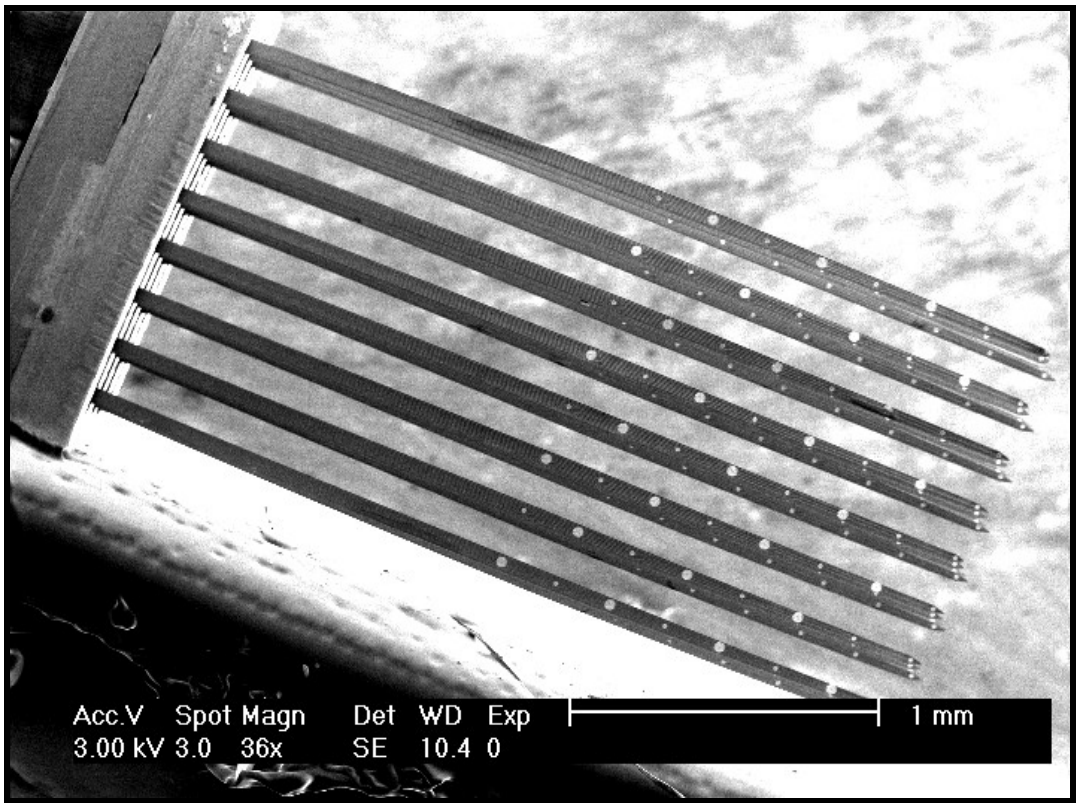


Fig. B.13: Conceptual drawing of the 256-site universal 3-D array.



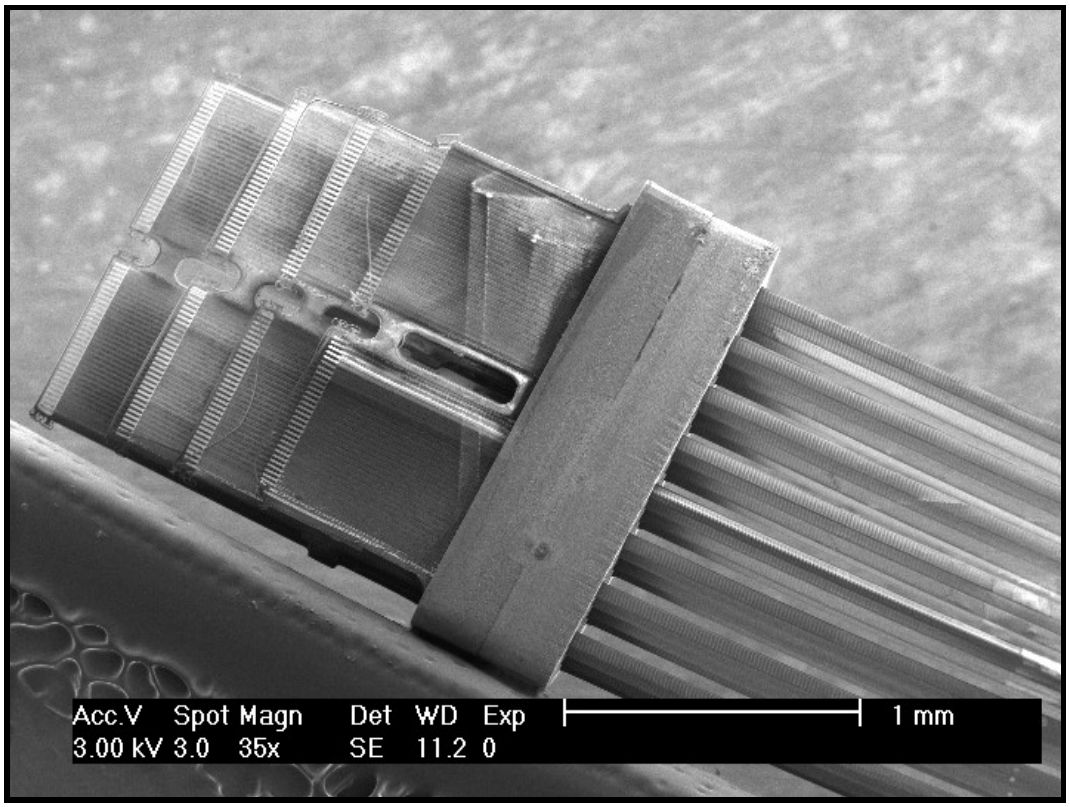




Fig. B.14: SEMs of the electrode array shanks (top) with large and small sites and of the staggered length integrated cables with beam-lead termination (bottom).

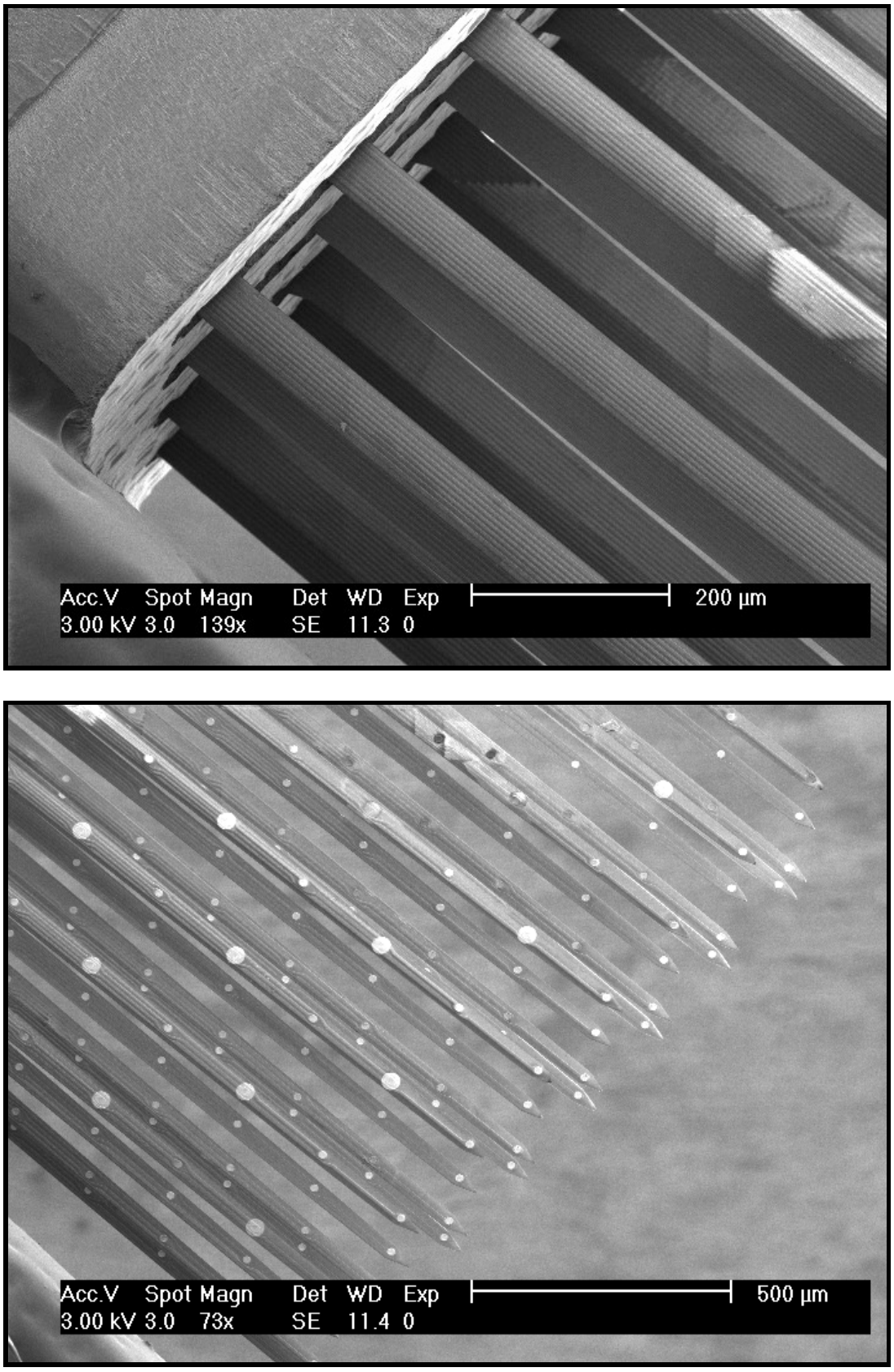



Fig. B.15: SEM close-ups of the 256-site array.

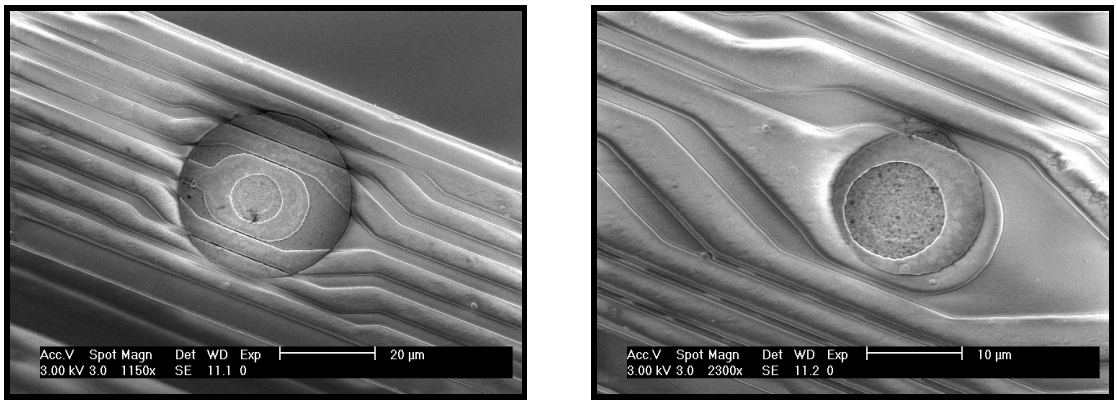



Fig. B.16: SEMs showing 1000µm$^2$ (left) and 177µm$^2$ (right) electrode sites.

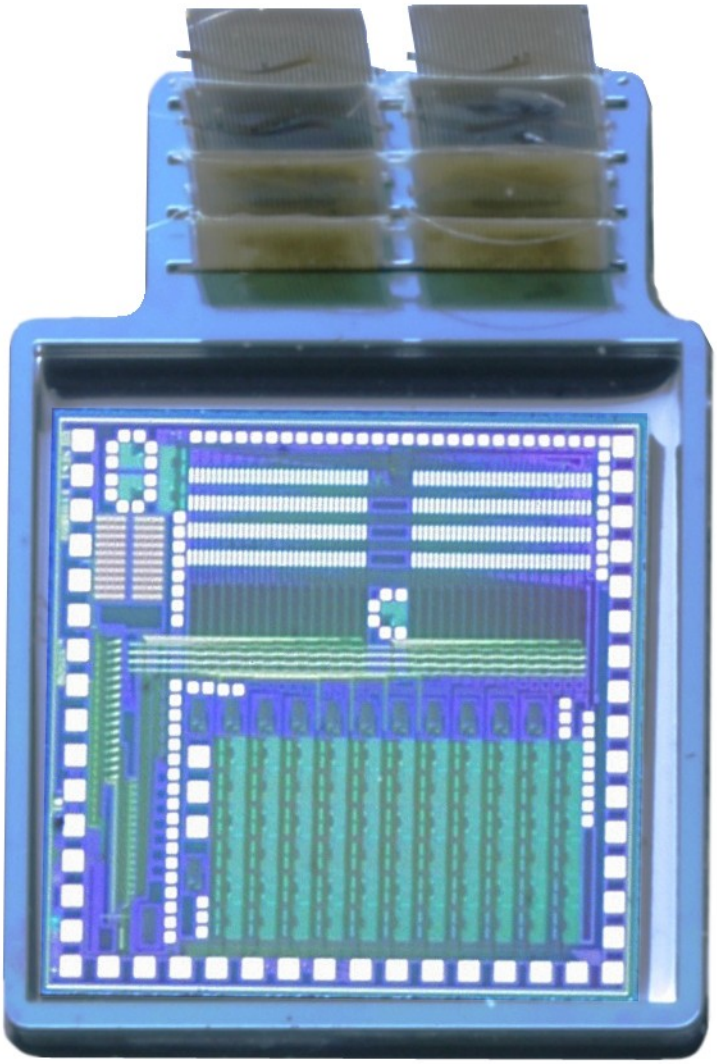


Fig. B.17: Cut-out photograph of a test chip for the R/S ASIC in a silicon platform with four electrode array probes before the integrated probe cables are folded down. Optimization of fine-pitch beam-lead bonding is necessary before finalizing this integration method.

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When recording neural signals several things must be accounted for, including the background noise or field potentials and the typical firing rate without stimulus of a particular channel. Therefore, the stimulus is started some milliseconds into the recording time frame and ends before the end of the frame. A recording block includes the repetition of frames in order to obtain statistically relevant information on spike count during the stimulus in comparison to that before or after the stimulus. The neural responses are recorded as waveform voltage over time. Real-time signal processing software is used so that the signals and particular features can be observed during the study and so immediate decisions can be made during the experiment. First the thresholds of each channel are set, automatically or manually, in order to determine the voltage levels beyond which a signal will be counted as a neural spike. Once thresholding has been completed, spike clips are overlaid, spike rasters are charted, and histograms plotted. The post-stimulus time histogram (PSTH) is one of the main visualization tools for immediate verification of responses. The time frame is divided into small time bins; the per bin spike count of the repeated frames in a block summed and the total spikes per bin are plotted. Fig. 7.13 presents the PSTH recorded for one channel in response to an acoustic noise burst; the spikes per bin are significantly greater during the stimulus than either before or afterwards.

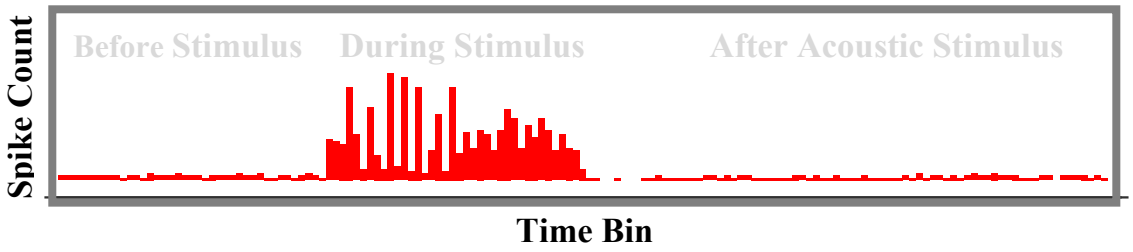


Fig. 7.13: Recorded PSTH of an elicited response due to a 70dB acoustic noise burst.

When stimulated with a tone at its characteristic frequency, the corresponding PSTH of a CN cell is one indicator of cell type. Fig. 7.14 shows sketches of the distinguishing shape of PSTHs for five main CN cell types from both subdivisions. A spread of patterns has been observed from recordings with the VCN-DCN arrays; a selection of these responses is presented in Fig. 7.15 for both subnuclei. In this work, typically characteristic PSTHs were recorded with 500 repetitions at a sound level 20dB above the threshold of the unit.